Contemporary Mathematics
http://ojs.wiserpub.com/index.php/CM/

UNIVERSAL WISER PUBLISHER

Research Article

# An Improved Z-Source Inverter Topology with Fewer Passive Components: Hardware Validation and Modelling

**Tushar Tyagi[1*], Amit Kumar Singh[1], Himanshu Sharma[1], Rintu Khanna[2]**

[1]School of Electronics and Electrical Engineering, Lovely Professional University, Phagwara, Punjab, India
[2]Department of Electrical Engineering, Punjab Engineering College, Chandigarh, India
Email: tushar.20586@lpu.co.in

**Received:** 5 June 2023; **Revised:** 7 August 2023; **Accepted:** 22 August 2023

**Abstract:** This research investigated a novel Z-source inverter architecture with fewer passive components. The offered inverter has several advantages, including low-frequency switching at 50 Hz, a straightforward modulation technique, and a constant input current. Low switching frequency results in fewer switching losses, which improves the overall efficiency of the inverter. The adoption of a straightforward modulation method allows for more exact control of the output voltage frequency. Because of these qualities, this inverter architecture can be employed in solar applications. This provides a thorough examination of shoot-through and non-shoot-through modes. The comprehensive mathematical underpinning of various modes is described here, and the established mathematical equations are shown to be consistent with the simulation. The number of components, which is only four in number, switching frequency, and boost factor of the presented topology prototype are compared to various well-known topologies in the literature. The power density of the inverter is 25% higher than the topology having the fewest number of components as reported till date for a single-phase Z-source inverter. Finally, a laboratory prototype is created to corroborate the analysis and validation of the data reported by the MATLAB simulation.

***Keywords*:** inverter, Z-source inverter, shoot-through, boost factor

**MSC:** 91B74, 93A30, 97M10, 00A71

## 1. Introduction

Significant research efforts are being conducted across the world in the fields of renewable energy conversion, electrical transportation, and a variety of other industrial uses that need power converters or inverters. As a result, there is enormous potential for building economically viable, technically possible, efficient, and dependable power converters [1-3].

For short-circuit protection, a dead period is necessary between switches of the same branch in a typical inverter, resulting in distortion of the alternating output voltage waveform. The overall efficiency of the whole system reduces when introducing an intermediary DC-DC conversion stage for a weak DC source voltage. The aforementioned issues pushed power electronics experts to have a conversion in only one step without sacrificing the boost of the input voltage and, therefore, having good overall efficiency [1, 4, 5]. The Z-source inverter (ZSI) was introduced for the first time


DOI: https://doi.org/10.37256/cm.5320243165

in 2002 [1]. In Figure 1, the circuit design depicts an impedance network in the shape of an X with two capacitors and two inductors that allow buck-boost operation in the single-stage conversion of input power. In ZSIs, power electronic switches connected in the same branch may be switched on at the same time without jeopardising the stability and accurate operation of the inverter.

The last decade has seen huge progress in the development of the different topologies for ZSIs. At one end, the researchers concentrated on modulation tactics, uses in the field of technology, and modelling [6, 7], while others worked on developing novel topologies. The majority of the work is done for three-phase ZSIs, but a substantial focus is required for the development of single-phase ZSIs in low-power or micro-renewable energy systems. This work proposes a new single-phase, half-bridge ZSI architecture for renewable energy applications.

In [8], a design with qualities comparable to ZSI but with fewer passive components is proposed; nonetheless, because of the increased count of active devices, the switched boost inverter (SBI) requires a superior protection circuit than ZSI. SBI's typical DC-link voltage is just one-tenth of that of ZSI. Topologies presented in [9] offer an elevated boost factor when compared to traditional types, with fewer counts of passive components and high efficiency when compared to standard ZSI. After that, a better half-bridge switched boost inverter (HB-SBI) design has been proposed with reduced voltage pressure on capacitors [10]. In comparison to the half-bridge ZSI with two Z-networks, the suggested half-bridge quasi-switched boost inverter (HB-QSBI) features fewer passive components. Furthermore, as compared to standard topologies, the suggested topology provides a high voltage gain and operates in a stable region. The topology presented in [11] offers buck-boost capabilities as well as dual grounding. Moreover, the suggested inverter has a larger voltage gain than the quasi-Z-source inverter (QZSI) and semi-ZSI. However, this topology contains many passive elements.

Lashab et al. [12] proposed a dual-input QZSI for photovoltaic applications. This topology intends to get greater power out of solar panels [12]. Iijima [13] proposes a novel switching approach for a ZSI with asymmetrical shoot-through durations to eliminate the current ripple in its connected inductors. This method offers an inductor current ripple reduced by 26.9% compared to a conventional scheme with equivalent shoot-through intervals.

For the reduction of losses, [14] proposes a new sinusoidal modulation approach. The successful implementation of the sinusoidal modulation approach is validated using a prototype. In [15], various boost inverter topologies are discussed for very small grid applications while having only single-stage power conversion. In [16], a new layout for ZSIs based on the switching boost network (SBN) is proposed. The inverter in [16] is known as a dual-switched boost inverter (DSBI). DSBI uses two cascaded switched networks to raise the SBI's boost factor. One of the most essential features of DSBI is that the proposed structure can be constructed even if the switched boost network is accessible as a block with two I/O terminals. In [17], an extension of the quasi-switched boost inverter (QSBI) termed a high-gain quasi-switched boost inverter (HG-QSBI) is presented. The boost factor of HG-SBI is 1/(1-3D) as compared to 1/(1-2D), providing higher gain as compared to the QSBI. The input current of the inverter is continuous, and the modulation strategy is similar to that of QSBI. However, the component count is higher than QSBI. In [18], the family of enhanced boost QZSI inverter topologies is proposed, which have a high boost factor at a high modulation index and improved output voltage waveform quality. In [19], a thorough investigation of multiport DC-DC converters is presented with the latest research findings in the area. The mentioned multiport DC-DC converters are best suited for renewable energy applications and electric vehicles. A detailed classification and characteristics of the multi-port converters are presented in [20] to address the issues of voltage synchronisation and protection during the integration with the microgrid.

In this article, a new ZSI topology with fewer passive components is developed. The topology is suitable for use in photovoltaic applications. The switching frequency is kept at 50 Hz, which is very low compared to the switching frequency used in the topologies proposed in [1, 8-10]. The low-frequency results in the higher efficiency of the inverter. The modulation technique used to generate the gate pulses for the switches is simple and easier to implement. Different modes of the inverter are discussed in detail, and the analysis for the same is also carried out. The laboratory prototype developed is in close agreement with the simulation developed and confirms the superiority of the proposed topology in photovoltaic or low-power applications. The main advantages of the proposed topology are low switching frequency, smaller size, high efficiency, and continuous current.

The organisation of the rest of the paper follows as Section 2 presents the proposed inverter topology along with different operating modes. Performance characteristics of the proposed inverter topology are discussed in Section 3. The results and discussion, along with validation of simulation results with hardware, are presented in Section 4. The

conclusion of the research work has been described in Section 5.

## 2. Proposed topology

Two inductors (L1 and L2), two switches (S1 and S2), two sources, and one capacitor are used to realise the proposed topology. In comparison to the standard ZSI topology as depicted in Figure 1, which is composed of fewer counts of active and passive elements, the circuit diagram is depicted in Figure 2. The circuit draws a continuous current, which is an advantage of the topology under consideration.

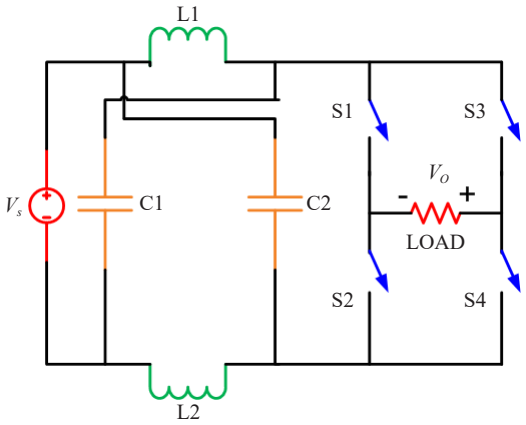



**Figure 1.** Z-source topology

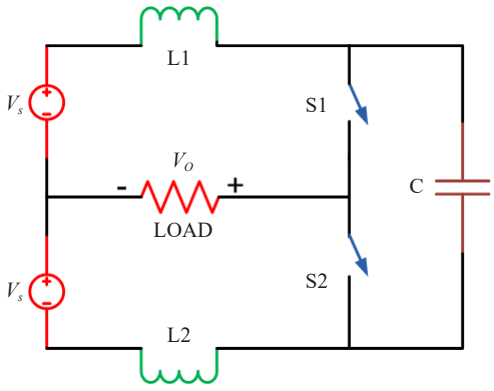



**Figure 2.** Proposed topology

### 2.1 *Operating modes*

The proposed topology has four operating modes. The following sections discuss the various switching states as well as a detailed analysis of the topology.

#### 2.1.1 *Circuit operation mode 1: When S1 and S2 are ON*

The inverter is said to be in a shoot-through state where S1 and S2 are closed for the duration of $DT_s\frac{T_s}{2}$ where $DT_S$

is the duty ratio and $T_s$ is the switching time period. The inductor charges in this mode. When selecting the capacitor's value, caution should be exercised because the capacitor's value will determine the inrush current at start-up. Figure 3 depicts an equivalent circuit for this mode. The inrush current depends on the value of the capacitor used. In the proposed topology, the selection of the capacitor is carried out by the hit-and-trial method by using different values and keeping close observation of the inrush current. Finally, the value of a capacitor is decided based on the trade-off between inrush current and boosting voltage.

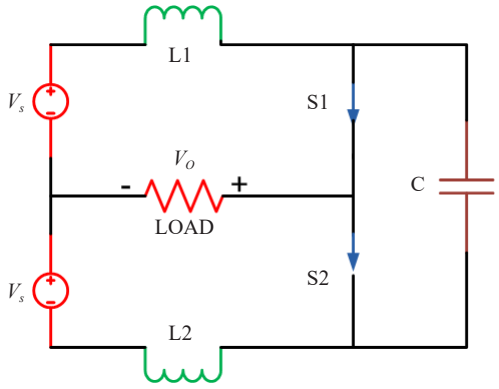



**Figure 3.** Shoot-through state

### 2.1.2 *Circuit operation mode 2: When S1 is ON and S2 is OFF*

In mode 2, the inverter is said to be in non-shoot-through mode for the duration of $1 - DT_s\frac{T_s}{2}$. In this mode, switches' states are 1 and 0 for S1 and S2, respectively, as shown in Figure 4. While the inductor is discharging and the inductor's voltage is summed up to the source voltage, the output voltage is boosted. The comparable circuit is depicted in Figure 5.

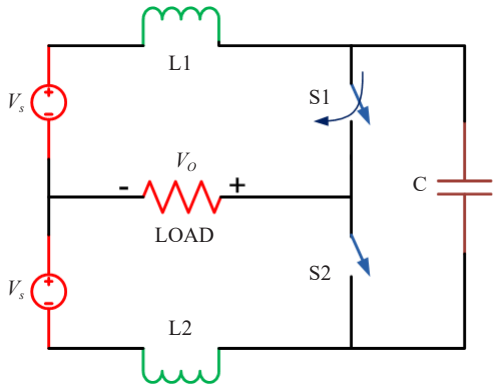



**Figure 4.** Mode 2 circuit diagram

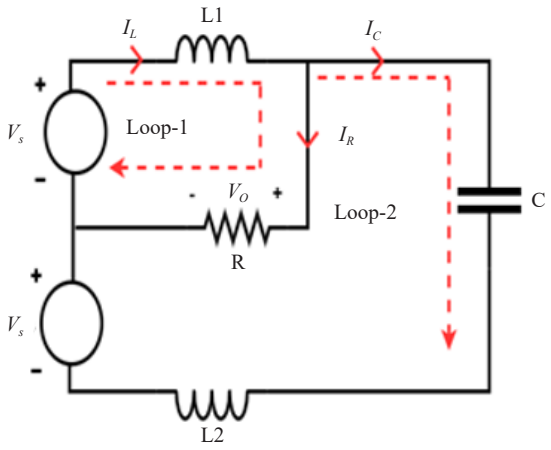



**Figure 5.** Mode 2 equivalent circuit

Voltage and current relations:

$$I_{L1} = I_R + I_C \tag{1}$$

$$V_s = V_{L1} + V_O \tag{2}$$

After applying the Kirchhoff's voltage law (KVL) in loop-1 for the duration of $\frac{DT_s}{2} < t < \frac{T_s}{2}$, we get

$$V_s = L * \frac{dI_{L1}}{dt} + R * I_R \tag{3}$$

$$I_{L1} = I_R + I_C \tag{4}$$

Putting the value of $I_{L1}$ in equation (3), we get

$$V_s = L * \frac{d(I_R + I_C)}{dt} + R * I_R \tag{5}$$

$$V_s = L * \frac{dI_R}{dt} + L * \frac{dI_c}{dt} + R * I_R \tag{6}$$

$$V_s - L * \frac{dI_R}{dt} - L * \frac{dI_c}{dt} - R * I_R = 0 \tag{7}$$

Taking the Laplace transform of the equation (7) assuming zero initial condition,

$$\frac{V_s}{s} - sL * I_R(s) - sL * I_C(s) - R * I_R(s) = 0 \tag{8}$$

$$(s^2 * L + s * R) * I_R(s) + s^2 * L * I_C(s) = V_s \tag{9}$$

Now, applying the KVL in loop-2

$$V_s + R * I_R + \frac{1}{C}\int I_C dt - L * \frac{dI_C}{dt} = 0 \tag{10}$$

Taking the Laplace transform of equation (10), we get

$$\frac{V_s}{s} + R * I(s) + \frac{1}{C} * \frac{I_C(s)}{s} - s * L * I_C(s) = 0 \tag{11}$$

$$I_R(s)(s * R * C) + (1 - s^2 * L * C) * I_C(s) = -C * V_s \tag{12}$$

Solving equations (9) and (12) for $I_C(s)$ we get

$$I_C(s) = \frac{C * v_s(R + s * L)}{s^3 * L^{2*} C + s^2 * 2 * R * L * C + s * L + R} \tag{13}$$

Taking inverse Laplace after putting the value of $C = 120\ \mu F$, $R = 10\ \Omega$, and $L = 9$ mH:
The approximate solution of the equation is

$$I_C(t) = 3 * e^{-\frac{625t}{3}} * \cos(647 * t) + 3.109 * \sin(647 * t) \tag{14}$$

The equation (14) has mainly two components: one is decaying with a frequency of 100 Hz, and the other is sinusoidal with a frequency of 100 Hz, which is consistent with the simulation and hardware results.

### 2.1.3 *Circuit operation mode 3*

This mode is similar to mode 1, and the inverter is again in the shoot-through state, where both switches are closed.

### 2.1.4 *Circuit operation mode 4: When S1 is OFF and S2 is ON*

In mode 4, switches' states are 0 and 1 for S1 and S2, respectively, as shown in Figure 6. While the inductor is discharging and the voltage across L2 is summed up to the source voltage, the output voltage is boosted, which is similar to mode 2 operation. The equivalent circuit for this mode is also presented in Figure 7.

Voltage and current relations:

$$I_L = I_R + I_C \tag{15}$$

$$V_s = V_{L2} + V_O \tag{16}$$

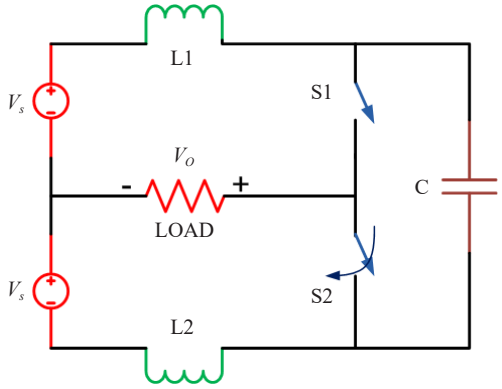



**Figure 6.** Mode 4 circuit

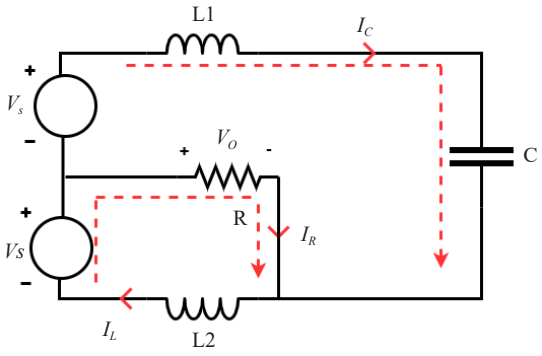



**Figure 7.** Mode 4 equivalent circuit

## 2.2 *Calculation for boost factor*

For boost factor calculation, the average voltage of the inductor over time is made equal to zero. In mode 1, apply KVL to the circuit. We get

$$V_s = V_{L1} \tag{17}$$

Similarly, now apply the KVL to the circuit of the mode 2 equivalent circuit. We get

$$V_{L1} = V_s - V_O \tag{18}$$

Now, equate the voltage-second balance of the inductor to zero.

$$\frac{D_{st} \times V_s}{2} + \frac{(1 - D_{st}) \times (V_s - V_O)}{2} = 0 \tag{19}$$

$$V_o = \frac{V_s}{1 - D_{st}} \tag{20}$$

$$B = \frac{1}{1 - D_{st}} \tag{21}$$

## 3. Performance characteristics

In this part, different performance characteristics for the proposed topology are examined. The parameters that are under observation are total harmonic distortion, output voltage, and boost factor. All these parameters are observed under variation of the $D_{st}$.

### 3.1 *Output voltage variation with $D_{st}$*

It is apparent from the expression of output voltage as given in (4) that by increasing $D_{st}$ the output voltage will rise, as depicted in Figure 8. The $D_{st}$ can be increased only up to a specific point; an additional increment in $D_{st}$ may result in an unreliable operation of the inverter.

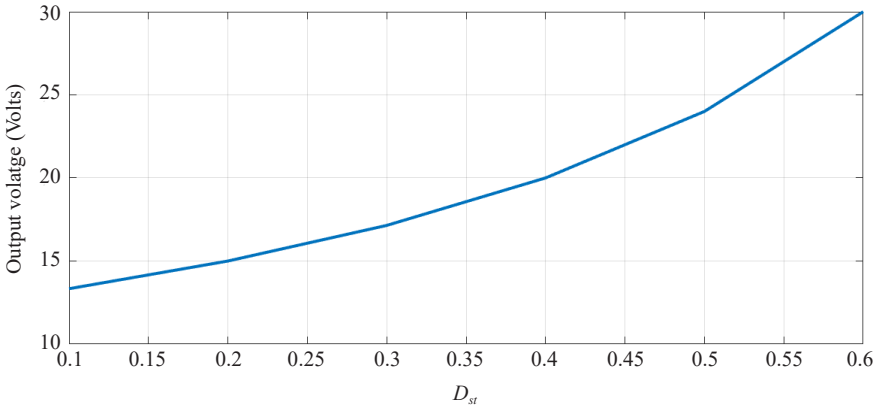



**Figure 8.** Output voltage variation with $D_{st}$

### 3.2 *Output voltage variation with boost factor*

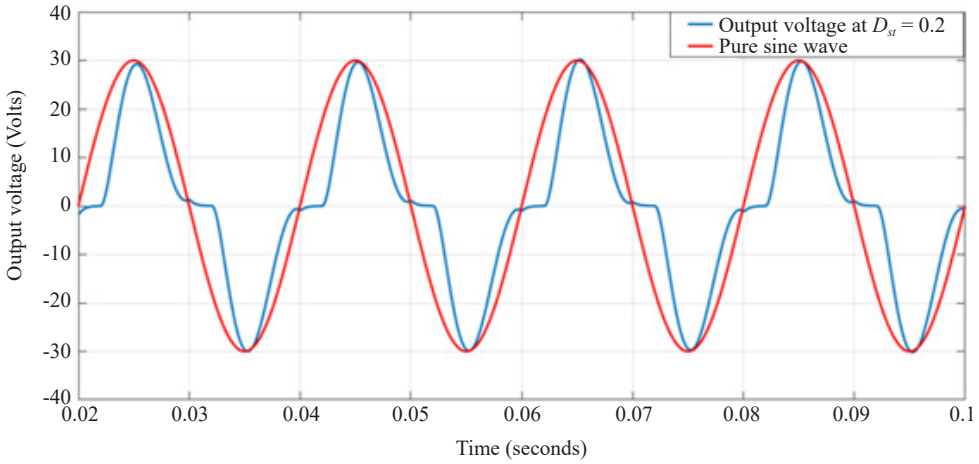



**Figure 9.** Pure sine wave voltage comparison with output voltage

As seen in Figure 9, the output voltage swells when the boost factor increases, but the waveform is distorted by the sine wave voltage. Because the duration of the shoot-through is so short, it will have little impact on the inverter's performance. Figure 10 depicts the voltage variation at $D_{st}$ = 0.2 and 0.3.

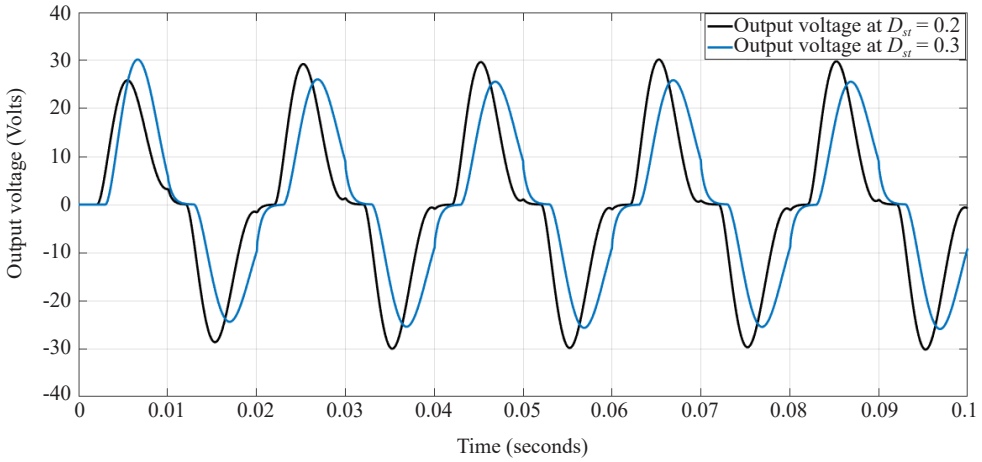


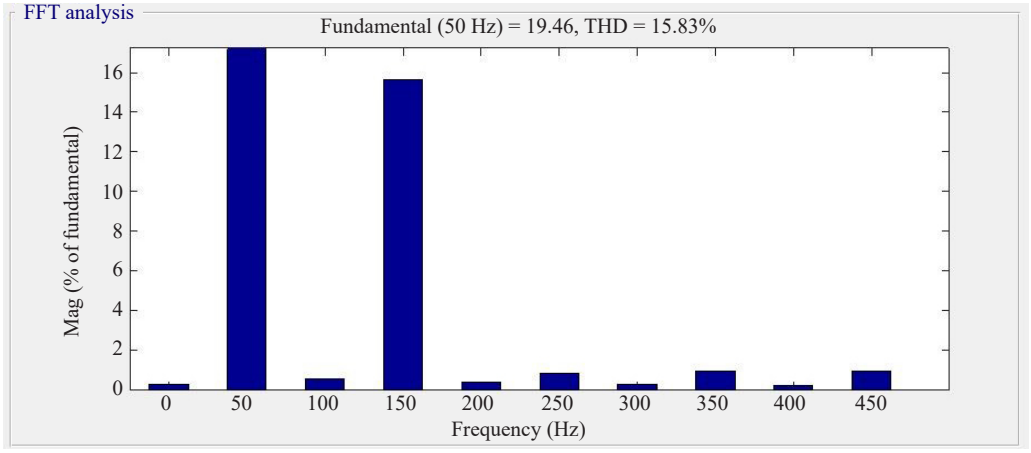

**Figure 10.** Variation of output voltage with $D_{st}$ = 0.2 and $D_{st}$ = 0.3

## 3.3 *Total harmonic distortion and boost factor variation*

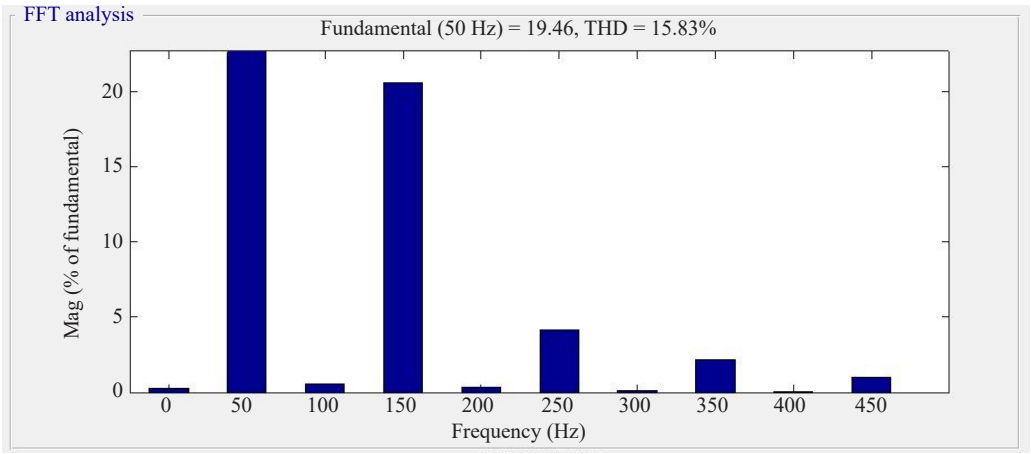
As indicated in Table 1, the total harmonic distribution (THD) value of the output voltage rises as $D_{st}$ is increased. THD increases as the output voltage diverges from the pure sine wave. Figure 11 shows the THDs determined by simulation and the power quality (PQ) analyser for $D_{st}$ = 0.1 and $D_{st}$ = 0.2. Figure 11 shows that the findings obtained by simulation and the PQ analyser are fairly close. The selection of DST depends on the preference given to power quality or boosting voltage. Hence, there will be a trade-off between THD and $D_{st}$.

**Table 1.** THD and boost factor variation

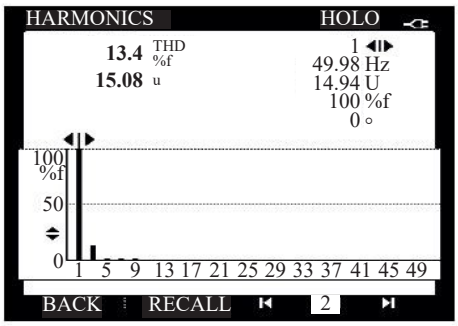
| $D_{st}$ (%) | Boost factor | THD (%) by simulation | THD (%) by PQ analyser |
|---|---|---|---|
| 4 | 1.04 | 12.86 | - |
| 10 | 1.11 | 15.83 | 13.4 |
| 20 | 1.25 | 21.16 | 20.2 |
| 30 | 1.43 | 27.38 | - |
| 40 | 1.67 | 36.91 | - |



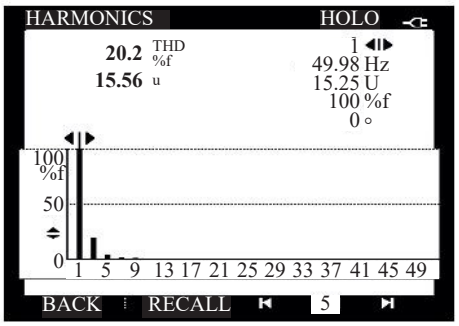

(a)




(b)




(c)




(d)

**Figure 11.** THD with (a) $D_{st}$ at 0.1 by simulation, (b) $D_{st}$ at 0.2 by simulation, (c) $D_{st}$ at 0.1 by PQ analyser, and (d) $D_{st}$ at 0.2 by PQ analyser

## 3.4 *Losses and efficiency*

In an inverter, there are mainly two types of losses: on-state losses and switching losses. In the proposed topology, there are only two switches, hence the on-state losses of the inverter are low; furthermore, due to the low switching frequency, the switching losses of the inverter have been reduced by a great deal, resulting in good overall efficiency as compared to other topologies.

# 4. Results and discussion

## 4.1 *Modulation strategy for generation of control signal*

The control signals to turn on and off the power electronic switches are created as per the strategy illustrated in Figure 12. The triangular signal is first equated to two steady signals, VST1 and VST2. The strength of the two signals is directly determined by the duration of the shoot-through duty ratio. At a shoot-through duty ratio of $D_{st}$ then VST1 = $D_{st}$, VST2 = 1 – $D_{st}$. By equating a sinusoidal signal to zero, a signal S is formed. S', on the other hand, is the complement of S. The inverter's output frequency is 50 Hz. The proposed inverter has the advantage of switching at a very low frequency, which decreases switching losses and boosts efficiency.

## 4.2 *Simulation results*

The topology under consideration is tested in Simulink by MATLAB to see how it performs and behaves under various loading circumstances. Figure 13 depicts the output voltage and its fluctuation with $D_{st}$. Figure 14 depicts the variation of capacitor current. The simulation shows that when $D_{st}$ increases, the inrush current of the capacitor drops while the root mean square (RMS) value of the output voltage increases.

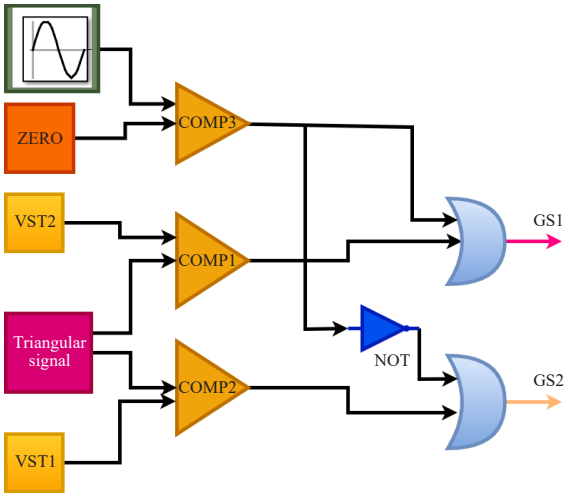



**Figure 12.** Gate signals for the switch

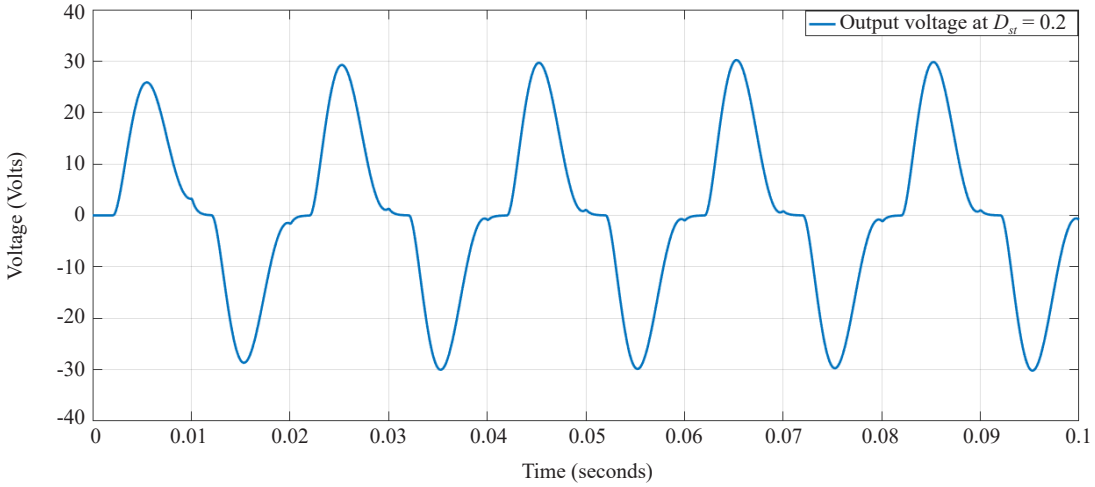
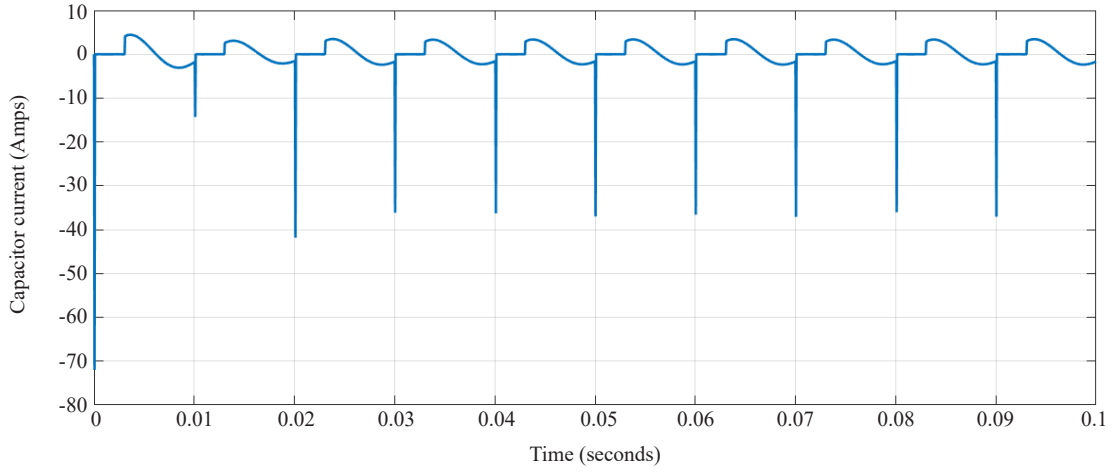
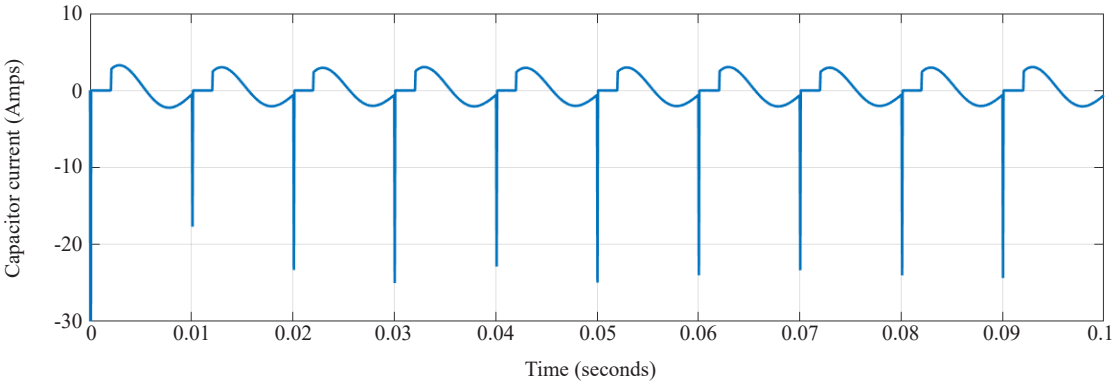


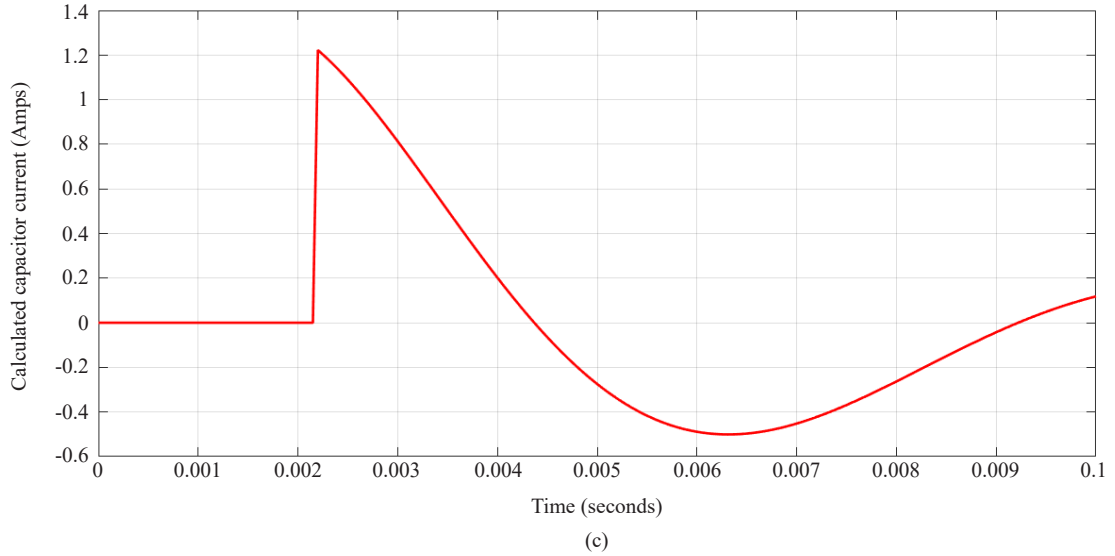

**Figure 13.** Output voltage waveform of the inverter




(a)




(b)

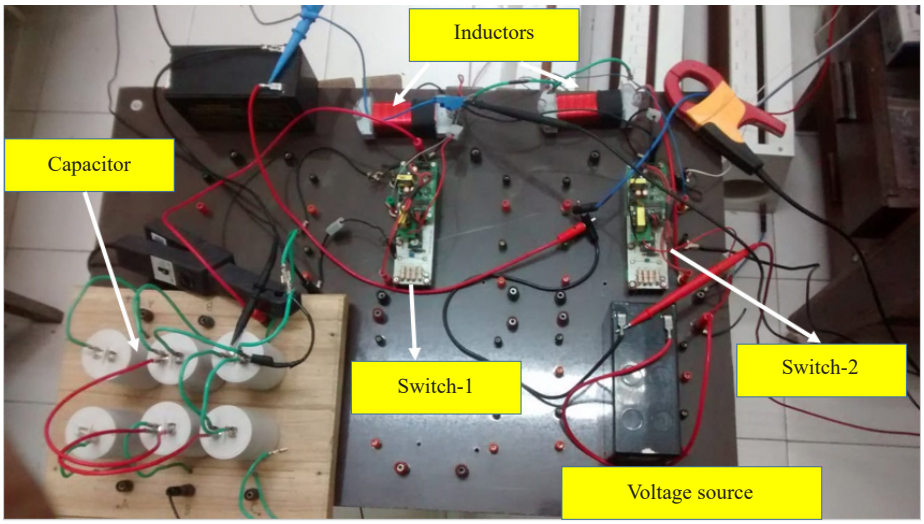



(c)

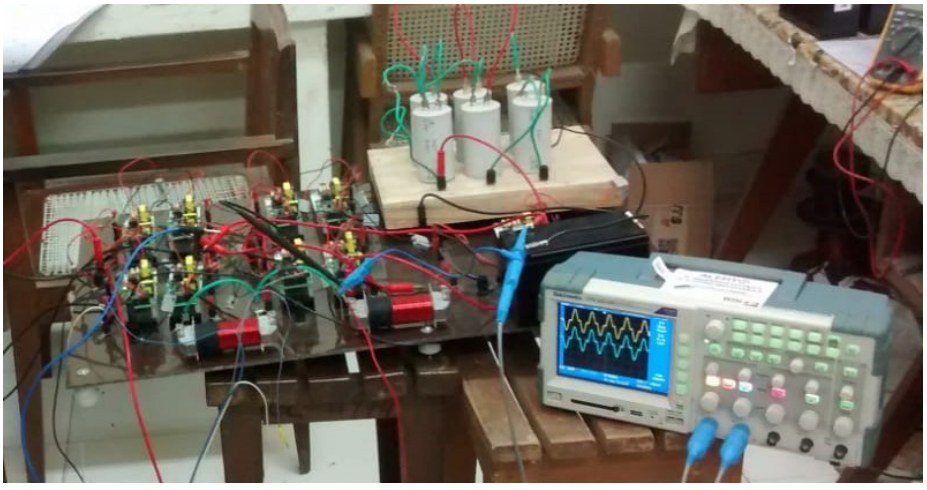
**Figure 14.** Variation of capacitor current (a) with $D_{st} = 0.2$, (b) with $D_{st} = 0.3$, and (c) calculated capacitor current as per equation (14)

## 4.3 *Experimental results*

The laboratory prototype of the proposed topology is developed and shown in Figures 15(a) and 15(b). The output voltage, capacitor current, capacitor voltage, and inductor voltage variations in real time are recorded and displayed. The gating signals for the switches are generated by the dSPACE using logic in Figure 12. Variation with boost factor and THD is also observed with the variation at $D_{st}$ = 0.1, 0.2, and 0.3, as shown in Figure 16.

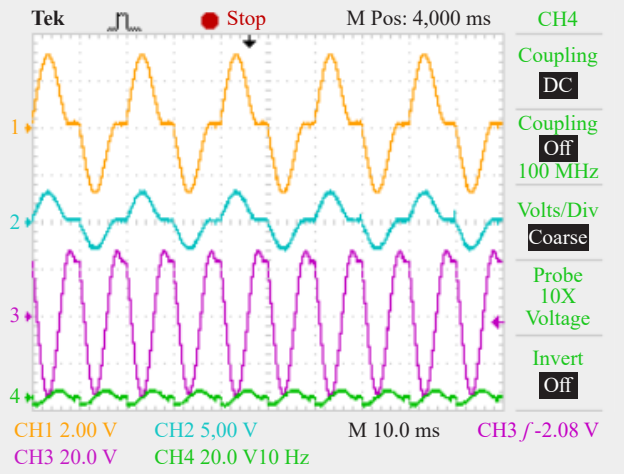



(a) The laboratory prototype

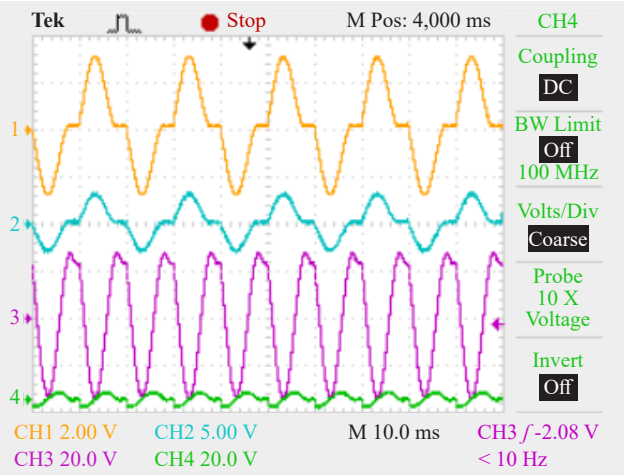


(b) The laboratory prototype

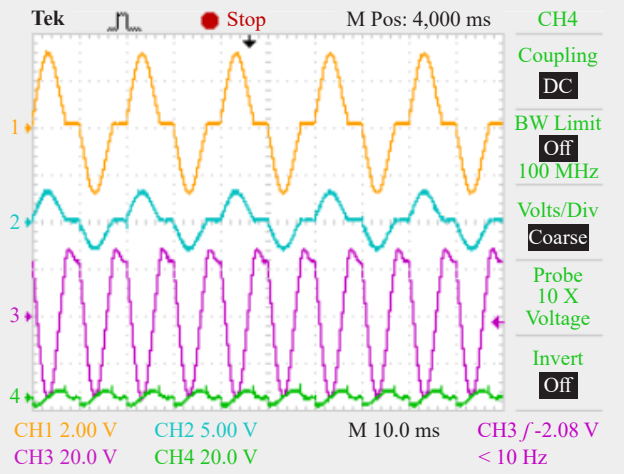
**Figure 15.** Variation of different parameters (a) with $D_{st}$ = 0.1, (b) with $D_{st}$ = 0.2, and (c) with $D_{st}$ = 0.3




(a)




(b)




(c)

**Figure 16.** Output voltage, current, capacitor voltage, and capacitor current at (a) $D_{st} = 0.1$, (b) $D_{st} = 0.2$, and (c) $D_{st} = 0.3$

## 4.4 *Comparative analysis*

The inverter under consideration is paralleled to recent times' topologies in the literature, and the comparison is drawn based on the component count as shown in Table 2. There are two inductors and two capacitors in the traditional ZSI design, but one less capacitor is being used in the proposed topology. Also, as the value of the capacitor decreases, the size of the inverter decreases. Another benefit of the topology is that the switching frequency is substantially low when compared to the conventional frequency, and the effect of a lower switching frequency results in the proposed inverter topology's high efficiency. Table 3 compares the number of components, switching frequency, and values of several passive components. There are several modulation strategies available for switching conventional ZSIs; however, many of them fail to maintain a consistent shoot-through duty cycle, affecting the inverter's performance. The modulation mechanism utilised here is straightforward, with a constant shoot-through duty ratio that may be modified as needed [21-23]. The circuit diagram of different topologies are shown in Figures 17-21. Where Figure 17 represents the circuit diagram of the SBI topology [8], Figure 18 represents the circuit diagram of the HB-SBI topology [9], Figure 19 represents the circuit diagram of the HB-QSBI topology [10], Figure 20 represents the circuit diagram of the QZSI topology [24], Figure 21 represents the circuit diagram of the CFSI topology [25].

**Table 2.** Components count in different topologies

| Topology | $N_L$ | $N_C$ | $N_S$ | $N_D$ | Power density (p. u.) | Boost factor | Circuit diagram |
|---|---|---|---|---|---|---|---|
| ZSI conventional [1] | 2 | 2 | 4 | 5 | 1/13 | $\frac{1}{1-2*D_{st}}$ | Figure 1 |
| SBI [8] | 1 | 1 | 5 | 1 | 1/8 | $\frac{1}{1-2*D_{st}}$ | Figure 17 |
| HB-SBI [9] | 1 | 2 | 4 | 6 | 1/13 | $\frac{1}{1-3*D_{st}}$ | Figure 18 |
| HB-QSBI [10] | 2 | 2 | 4 | 6 | 1/14 | $\frac{1}{1-2*D_{st}}$ | Figure 19 |
| QZSI [24] | 2 | 2 | 4 | 5 | 1/13 | $\frac{1-D_{st}}{1-2*D_{st}}$ | Figure 20 |
| CFSI [25] | 1 | 1 | 1 | 2 | 1/5 | $\frac{1}{1-2*D_{st}}$ | Figure 21 |
| Proposed topology | 1 | 1 | 2 | 0 | 1/4 | $\frac{1}{1-D_{st}}$ | Figure 2 |

**Table 3.** Comparative analysis

| Topology | $N_L$ | $N_C$ | $L$ (in mH) | $C$ (in µF) | Frequency (in Hz) | $N_D$ | $N_S$ |
|---|---|---|---|---|---|---|---|
| ZSI conventional [1] | 2 | 2 | 5 | 200 | 10,000 | 5 | 4 |
| SBI [8] | 1 | 1 | 5 | 100 | 10,000 | 1 | 5 |
| HB-SBI [9] | 1 | 2 | 4 | 25 | 10,000 | 6 | 4 |
| HB-QSBI [10] | 2 | 2 | 2.4 | 47 | 30,000 | 6 | 4 |
| Proposed topology | 1 | 1 | 9 | 120 | 50 | 0 | 2 |

For the comparison of power density, the following procedure is used:
Step 1: Let the power handled by the topologies used for comparison be 1 p.u.
Step 2: Let the volume of each component used be 1 p.u. as well.
Step 3: The power density is calculated using the equation below:

$$P_{den} = \frac{\text{Power of inventer}}{N_L + N_C + N_S + N_D} \tag{22}$$

where $N_L$, $N_C$, $N_S$ and $N_D$ is the number of inductors, capacitors, switches, and diodes respectively.

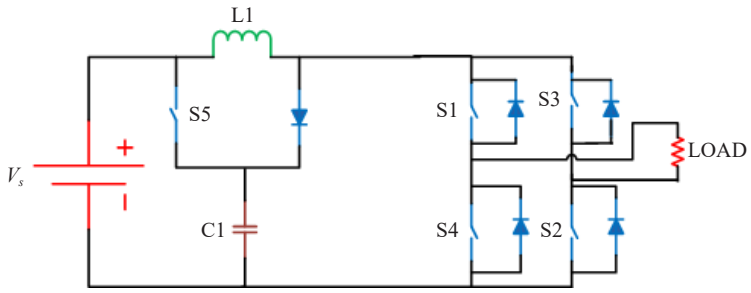



**Figure 17.** SBI

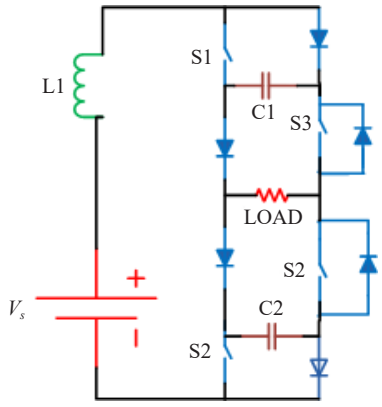



**Figure 18.** HB-SBI

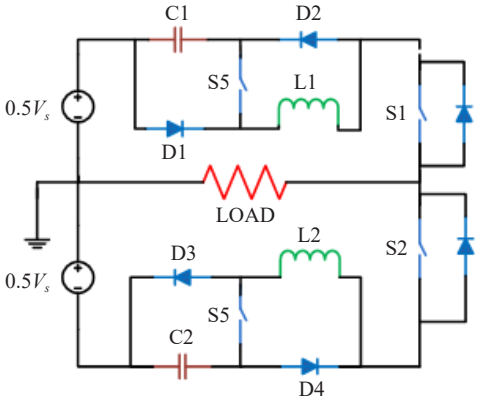



**Figure 19.** High voltage gain HB-QSBI

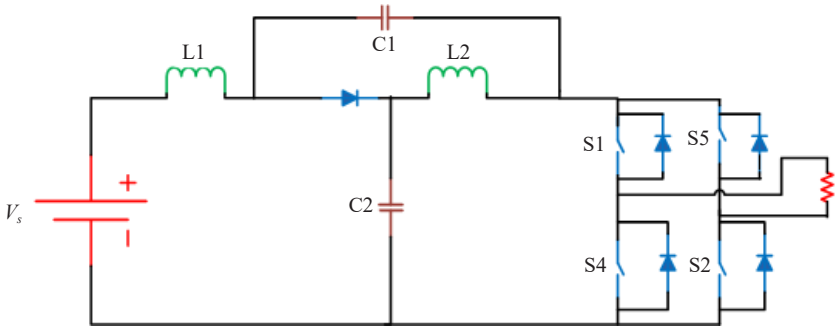



**Figure 20.** QZSI

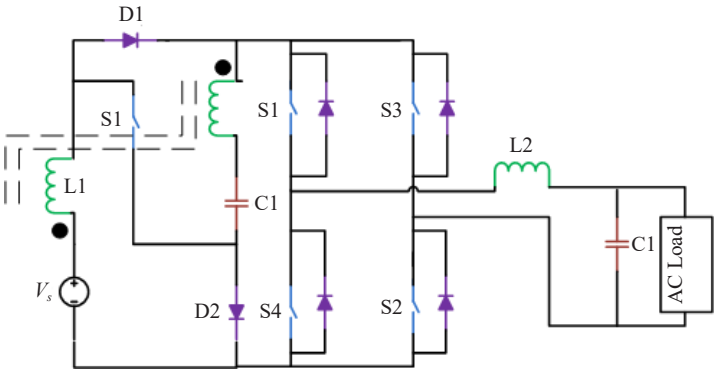



**Figure 21.** Current fed switch inverter

## 4.5 *Potential application*

The proposed topology can be used in applications where the input voltage is low but the requirement is much higher than the input without incorporating the stage in between. The solar farm is a potential application where the output voltage is low, but for some loads the requirement is much higher. The topology mentioned here can be used to boost the voltage without incorporating the intermediate stage. The possible block diagram for such an application is given in Figure 22.

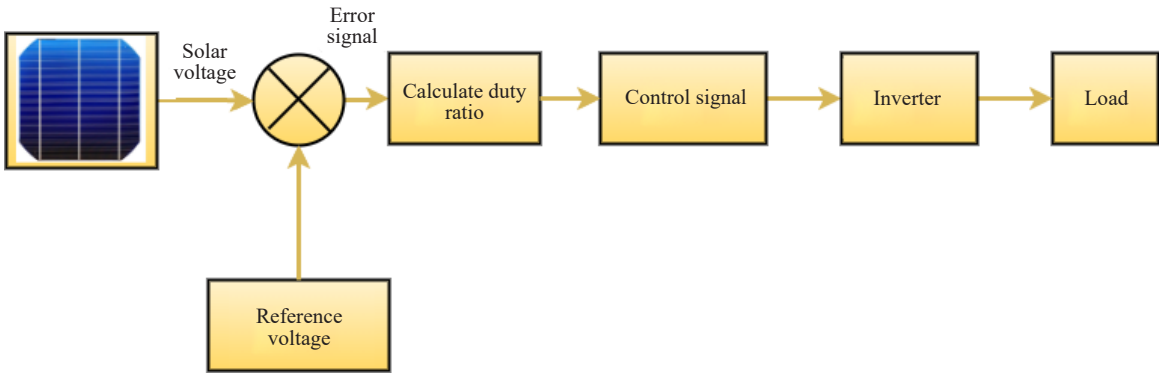
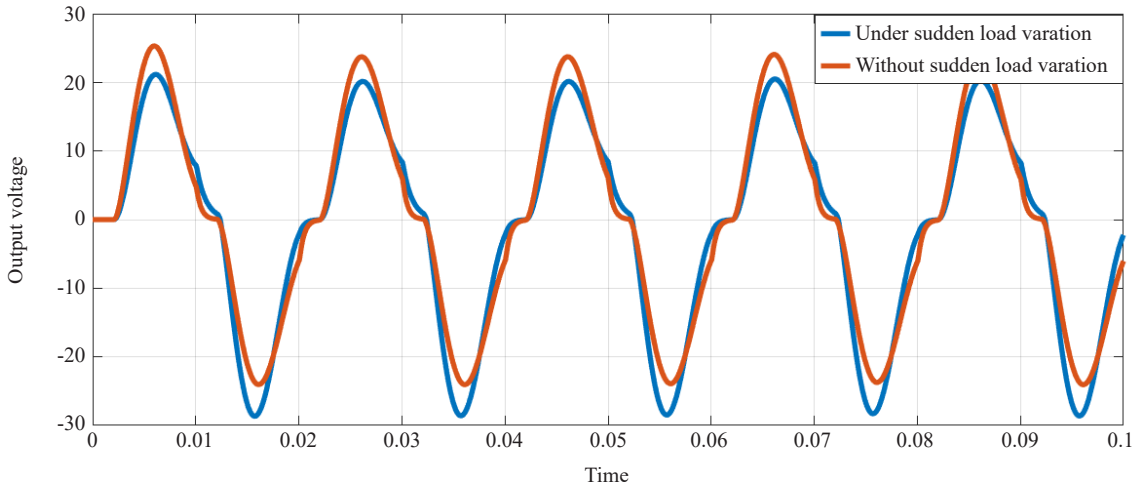


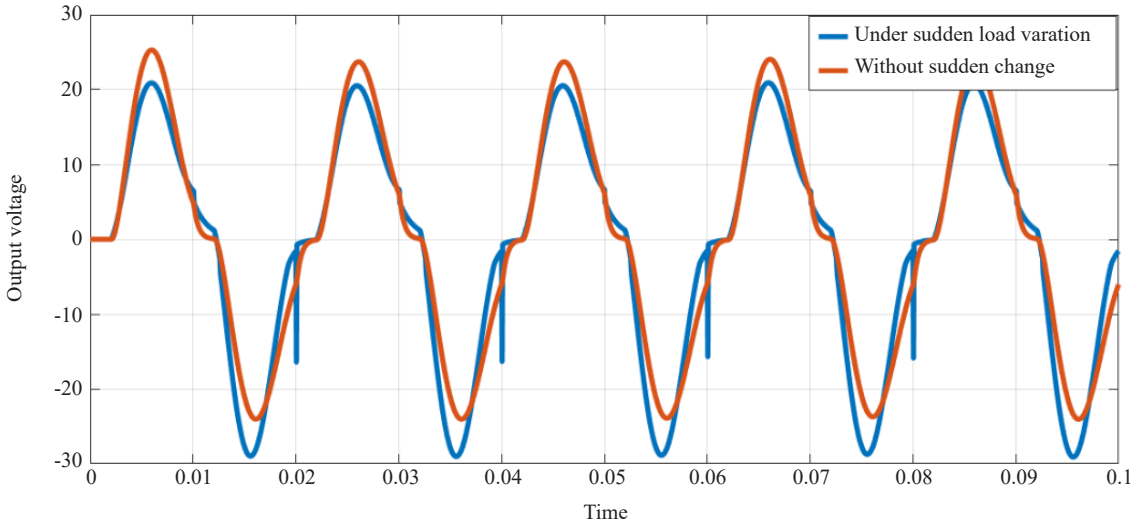

**Figure 22.** Block diagram for solar application of ZSI topology

## 4.6 *Stability under sudden load variation*

In order to check the stability of the proposed topology, it has been put under different sudden load variations. The stability of the output voltage is observed when the sudden resistive load and combination resistance-inductor (R-L) load are switched on. In the case of sudden R-L load variation, it was expected that there would be a distortion in the output voltage waveform, but overall, the effect of a sudden change in R-L is not substantial, hence it can be concluded that the topology is fairly stable in both conditions. The output voltage is stable under these two situations and is shown in Figures 23(a) and 23(b).




(a)




(b)

**Figure 23.** Variation of the output voltage under sudden change in (a) resistive load, and (b) R-L load

## 5. Conclusion

A novel ZSI topology with fewer passive components is introduced in this work. Both the switching and output frequencies are set to 50 Hz. Because of the lower switching frequency, the efficiency of the given inverter is better than that of traditional ZSI. The total size of the ZSI is reduced since there are fewer components. The many operating modes of the inverter are described and illustrated here. Different operating modes are theoretically modelled, and findings are validated using simulation results. The approach utilised to create control signals for the switches (modulation technique) is basic and easy to implement in hardware. The architecture, as well as numerous operating modes, are simulated in MATLAB, and a laboratory prototype is fabricated to confirm the simulation findings. The simulation findings produced here are fairly similar to the laboratory prototype results. Furthermore, the suggested inverter's input current is constant. When compared to certain previously discussed topologies in the literature, the topology differs based on parameters such as switching frequency and total number of components. The proposed inverter offers 1.25 times the power density based on the total number of four passive elements used to realise the stable operation of the inverter. The significant boost factor of 1.11 at 0.2 shoot through duty ratio with around 15% of THD is achieved without using any filter circuit. The best-suited application for the specification mentioned above is in a photovoltaic power conversion circuit. However, the architecture has several limitations. For example, operation beyond shoot-through duty ratio 0.5 is unstable since there is a chance of significant inrush current owing to the capacitor charging for a longer duration. Second, the overall harmonic distortion is considerable, which can be decreased further by adding appropriate load-side filters.

## Conflict of interest

The authors declare no conflict of interest.

## References

[1] Peng FZ. Z-source inverter. *IEEE Transactions on Industry Applications*. 2003; 39(2): 504-510. Available from: https://doi.org/10.1109/TIA.2003.808920.

[2] Yadav I. Load-line analysis of DC to DC converters for MPPT based solar PV applications. In: *2nd International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC)*. IEEE; 2022. Available from: https://doi.org/10.1109/PARC52418.2022.9726666.

[3] Yadav I, Maurya SK. The non-isolated DC to DC converters for MPPT controller based on the load line analysis used for solar PV applications. In: *Emerging Trends in Industry 4.0 (ETI 4.0)*. India: IEEE; 2021. Available from: https://doi.org/10.1109/ETI4.051663.2021.9619311.

[4] Badhoutiya A, Chandra S, Goyal S. Comparative evaluation of modulation schemes applied for PV connected Z-source inverter. In: *International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT)*. India: IEEE; 2020. p.164-168. Available from: https://doi.org/10.1109/RTEICT49044.2020.9315666.

[5] Badhoutiya A, Chandra S, Goyal S. Identification of suitable modulation scheme for boosted output in ZSI. In: *2020 4th International Conference on Electronics, Communication and Aerospace Technology (ICECA)*. Coimbatore, India: IEEE; 2020. p.238-243. Available from: https://doi.org/10.1109/ICECA49313.2020.9297633.

[6] Peng FZ, Shen M, Qian Z. Maximum boost control of the Z-source inverter. *IEEE Transactions on Power Electronics*. 2005; 20(4): 833-838. Available from: https://doi.org/10.1109/TPEL.2005.850927.

[7] Shen M, Wang J, Joseph A, Peng FZ, Tolbert LM, Adams DJ. Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. *IEEE Transactions on Industry Applications*. 2006; 42(3): 770-778. Available from: https://doi.org/10.1109/TIA.2006.872927.

[8] Ravindranath A, Mishra SK, Joshi A. Analysis and PWM control of switched boost inverter. *IEEE Transactions on Industrial Electronics*. 2013; 60(12): 5593-5602. Available from: https://doi.org/10.1109/TIE.2012.2230595.

[9] Asl ES, Babaei E, Sabahi M, Nozadian MHB, Cecati C. New half-bridge and full-bridge topologies for a switched-boost inverter with continuous input current. *IEEE Transactions on Industrial Electronics*. 2018; 65(4): 3188-3197. Available from: https://doi.org/10.1109/TIE.2017.2752118.

[10] Asl ES, Babaei E, Sabahi M. High voltage gain half-bridge quasi-switched boost inverter with reduced voltage stress on capacitors. *IET Power Electronics.* 2017; 10(9): 1095-1108. Available from: https://doi.org/10.1049/iet-pel.2016.0291.

[11] Wang B, Tang W. A new CUK-based Z-source inverter. *Electronics*. 2018; 7(11): 313. Available from: https://doi.org/10.3390/electronics7110313.

[12] Lashab A, Sera D, Martins J, Guerrero JM. Dual-input quasi-Z-source PV inverter: Dynamic modeling, design, and control. *IEEE Transactions on Industrial Electronics.* 2020; 67(8): 6483-6493. Available from: https://doi.org/10.1109/TIE.2019.2935927.

[13] Iijima R, Isobe T, Tadano H. Optimized short-through time distribution for inductor current ripple reduction in Z-source inverters using space-vector modulation. *IEEE Transactions on Industry Applications*. 2019; 55(3): 2922-2930. Available from: https://doi.org/10.1109/TIA.2019.2898848.

[14] Abdelhakim A, Blaabjerg F, Mattavelli P. Single-phase quasi-Z-source inverters: Switching loss reduction using a quasi-sinusoidal modulation strategy. In: *IEEE Applied Power Electronics Conference and Exposition (APEC).* IEEE; 2019. p.1918-1925. Available from: https://doi.org/10.1109/APEC.2019.8721955.

[15] Sriramalakshmi P, Sreedevi VT. Single-stage boost inverter topologies for nanogrid applications. In: SenGupta S, Zobaa A, Sherpa K, Bhoi A. (eds.) *Advances in smart grid and renewable energy.* Singapore: Springer; 2018. p.215-226. Available from: https://doi.org/10.1007/978-981-10-4286-7_21.

[16] Nozadian MHB, Babaei E, Ranjbarzad V. Steady state analysis of dual switched boost inverter. In: *IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018).* Qatar: IEEE; 2018. Available from: https://doi.org/10.1109/CPE.2018.8372572.

[17] Ye Y, Xu S, Chen S, Wang X, Cao L. High-gain quasi-switched boost inverter with single inductor and continuous input current. *IEEE Transactions on Power Electronics*. 2022; 37(9): 10106-10111. Available from: https://doi.org/10.1109/TPEL.2022.3166805.

[18] Jagan V, Alpuri MKR, Neeharika M, Swetha C, Mahendar P, Das S. A family of switched-impedance network enhanced-boost quasi-Z-source inverters. *International Journal of Power Electron and Drive Systems.* 2022; 13(1): 309. Available from: http://doi.org/10.11591/ijpeds.v13.i1.pp309-321.

[19] Gevorkov L, Domníguez-Garcaí JL, Romero LT, Martníez ÀF. Modern multiport converter technologies: A

systematic review. *Applied Science*. 2023; 13(4): 2579. Available from: https://doi.org/10.3390/app13042579.

[20] Gevorkov L, Domníguez-Garcaí JL, Martínez ÀF. Modern trends in multiport converters: Isolated, non-isolated, and partially isolated. In: *IEEE 63th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*. Latvia: IEEE; 2022. Available from: https://doi.org/10.1109/RTUCON56726.2022.9978910.

[21] Tang Y, Xie S, Zhang C. An improved Z-source inverter. *IEEE Transactions on Power Electronics*. 2011; 26(12): 3865-3868. Available from: https://doi.org/10.1109/TPEL.2009.2039953.

[22] Mohan N, Undeland TM, Robbins WP. *Power electronics: Converters, applications, and design*. 3rd ed. Wiley; 2002.

[23] Huang Y, Shen M, Peng FZ, Wang, J. Z-source inverter for residential photovoltaic systems. *IEEE Transactions on Power Electronics*. 2006; 21(6): 1776-1782. Available from: https://doi.org/10.1109/TPEL.2006.882913.

[24] Anderson J, Peng FZ. Four quasi-Z-source inverters. In: *IEEE Power Electronics Specialists Conference*. Greece: IEEE; 2008. p.2743-2749. Available from: https://doi.org/10.1109/PESC.2008.4592360.

[25] Nag SS, Mishra S. A coupled inductor based high boost inverter with sub-unity turns-ratio range. *IEEE Transactions on Power Electronics*. 2016; 31(11): 7534-7543. Available from: https://doi.org/10.1109/TPEL.2016.2543499.