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Review

Recent Advances of IGO-Based Thin-Film Transistors: A Review

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Abstract: Indium Gallium Oxide (IGO) Thin-Film Transistors (TFTs) are recognized as potential candidates to overcome current performance barriers and serve as a novel driving force for the next generation of commercial display technologies. Herein, we undertake a comprehensive overview of the performance optimization strategies for IGO-based TFTs. This review begins with a concise overview of the current landscape and prevailing challenges in TFTs. Then, it examines efforts to enhance the performance of IGO-based TFTs, with a particular focus on advances in active layer optimization, gate dielectric engineering, contact engineering, interface engineering, and device structure optimization. This review aims to provide a comprehensive resource for researchers working on IGO-based TFTs and related fields.

Keywords: thin film transistor, Indium Gallium Oxide (IGO), performance

1. Introduction

Thin-Film Transistors (TFTs) constitute the pivotal components in advanced display technologies, enabling precise control over individual pixels. Currently, the active-layer materials for commercially available TFTs mainly fall into three categories: Low-Temperature Polycrystalline Silicon (LTPS), amorphous Silicon (a-Si), and oxide semiconductors [1], [2]. However, LTPS suffers from complex fabrication processes, high cost, and poor uniformity, whereas the low carrier mobility of a-Si restricts its potential for next-generation display applications. As a result, considerable research efforts have been devoted to oxide-based TFTs, whose outstanding performance makes them highly promising for future advanced displays [3]-[5].

In the early stages of 2012, Taiwan's AUO and Chimei Technology made a significant transition, shifting their production lines to oxide-TFTs for mass-scale manufacturing. However, high defect densities, hysteresis characteristics and relatively elevated threshold voltages significantly diminish the effective field-effect mobility, thereby posing a considerable limitation on their practical utilization in display devices [6], [7]. Subsequently, through precise modulation of the oxide semiconductor composition, a-IGZO TFTs have emerged as promising candidates for various applications and have successfully made their way into commercialization [8]. Samsung pioneered the development of LTPO

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technology in 2018, the realization of which necessitates the integration of two distinct TFTs, namely an a-IGZO TFT and a polycrystalline silicon TFT, onto a single panel. While successfully addressing the leakage current issue associated with low-temperature polycrystalline silicon TFTs (Oxide semiconductors can reach extremely low turn-off current $\sim 1 \times 10^{-18}$ A μm^{-1}), this integration process remains both technically intricate and financially demanding [9]. In pursuit of superior performance and cost-efficiency for next-generation displays, the current limitations of a-IGZO TFTs and the considerable complexity of LTPO processes highlight the urgent need for further advancements and innovations in the realm of oxide TFT technology [10]-[13]. The precise incorporation of an optimal amount of Ga into In_2O_3 effectively mitigates off-state current and elevates device stability, thereby endowing Indium Gallium Oxide (IGO) TFTs with both outstanding performance and robust reliability. This combination positions IGO TFTs as a formidable contender for real-world technological applications [14]-[16]. In the last decade, researchers have devoted significant effort to improving the performance and fabrication processes of IGO-TFTs [17]. However, there is a lack of a comprehensive and specific review that encapsulates the advancements in this field.

Herein, we consolidate numerous recent studies on IGO-TFTs and provide a thorough analysis of their structural characteristics as well as the influence of key parameters on device performance. We systematically review the efforts devoted to performance enhancement, with particular emphasis on active-layer optimization—achieved through deposition-process control, doping, and post-treatment—and gate dielectric engineering, which encompasses material selection, thickness adjustment, structure design, doping optimization, and process refinement. Although research on contact engineering, interface engineering, and device-structure optimization remains relatively limited, innovations such as passivation treatment and double-layer structures indicate broad prospects for future exploration. This review comprehensively summarizes the current status and various optimization strategies for IGO-TFT performance, aiming to serve as a comprehensive reference for researchers working in this and related fields.

2. Performance optimization of IGO TFTs

We systematically scrutinize the endeavors made towards enhancing the performance of IGO TFTs, particularly focusing on advancements in active layer optimization, gate dielectric engineering, contact engineering, interface engineering, and device structure optimization, as summarized in Figure 1.

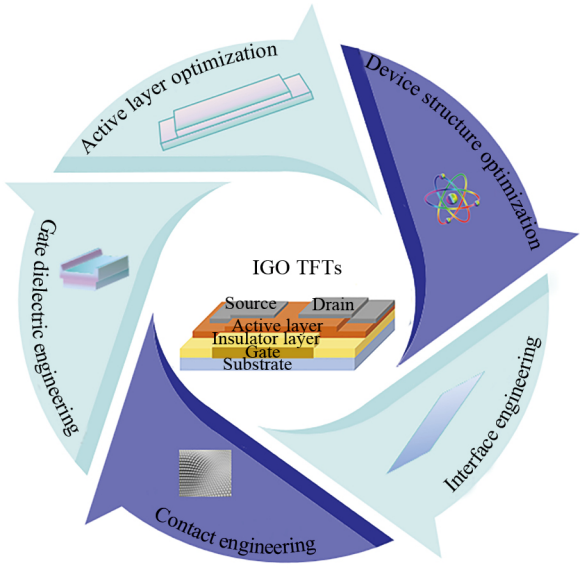


Figure 1. Methods to improve the performance of IGO TFTs

2.1 *IGO TFTs performance introduction and evaluation*

Understanding the operating characteristics of IGO TFTs is essential for effective device design and fabrication. These characteristics are obtained from current–voltage measurements, typically presented as transfer and output curves, from which key performance parameters are extracted. Figure 2 illustrates the standard transfer and output characteristic curves of an IGO TFT [18], [19].

Field-Effect Mobility (μ_{FE}): a key parameter that characterizes the average drift velocity of charge carriers per unit electric field, reflecting the ease with which carriers traverse the transistor channel. Higher mobility is highly desirable for TFT performance, as it enables lower power consumption and higher drive current, which in turn improves circuit speed and overall device efficiency. For instance, state-of-the-art IGO TFTs have demonstrated field-effect mobilities exceeding 100 cm^2 V^{-1} s^{-1} [20] through advanced engineering approaches, underscoring the significant performance gains attainable through mobility enhancement.

$$\mu_{FE} = \frac{L}{WC_iV_{ds}} \frac{\partial I_{ds}}{\partial V_{gs}}. \tag{1}$$

Threshold Voltage (V_{th}): The V_{th} is defined as the Gate Voltage (V_{gs}) at which the channel begins to conduct, corresponding to the midpoint of the sharp current-rise region in the transfer curve. A lower V_{th} is generally desirable as it reduces the operating voltage and power consumption; however, an excessively low V_{th} may lead to increased off-state leakage and standby power dissipation. To effectively reduce V_{th} while maintaining robust gate control, high-dielectric-constant (high-κ) gate dielectric materials are often employed, as they enhance the capacitive coupling between the gate electrode and the channel.

On-Off Current Ratio (I_{on}/I_{off}): The on-off current ratio is defined as the ratio of the maximum drain current in the on-state to the minimum drain current in the off-state under a fixed Drain-Source Voltage (V_{ds}). It serves as a key metric for evaluating the switching quality of a TFT. A higher I_{on}/I_{off} ratio indicates a clearer distinction between the on and off states, which is essential for reliable digital switching and low-power operation. The ratio is primarily determined by the off-state current, as the on-state current is typically limited by the channel mobility and device geometry.

Subthreshold Swing (SS): SS measures the V_{gs} required to increase the drain current by one decade in the subthreshold region, with units of mV dec^{-1}. It quantifies the steepness of the turn-on transition and reflects the device's switching efficiency. A smaller SS indicates faster switching and lower power consumption; the theoretical minimum at room temperature is approximately 60 mV dec^{-1} [21]. In practice, SS is strongly influenced by trap states within the active layer and at the interface between the active layer and the gate dielectric, as interface and bulk defects introduce additional charge trapping that degrades the subthreshold slope

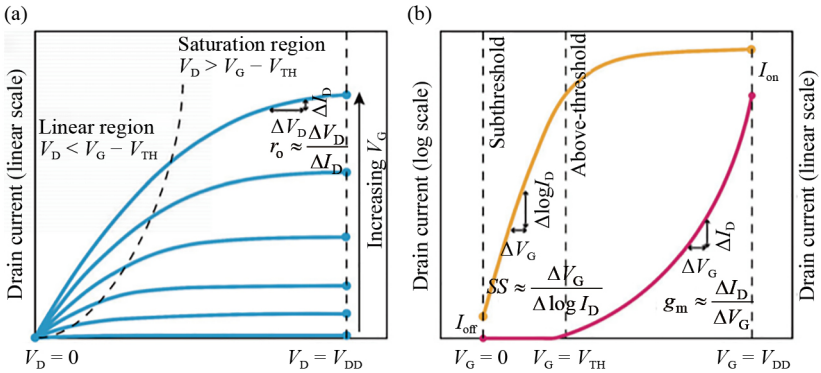


Figure 2. (a) Schematic illustration of output characteristics of a TFT. (b) Schematic illustration of transfer characteristics of a TFT and definitions of SS and g_m [22]

2.2 *Active layer optimization*

Current amplification and control in transistors fundamentally depend on the injection and modulation of charge carriers within the channel region. In TFTs, this critical function is realized by the semiconductor active layer, which serves as the channel [21]. To optimize the active layer of IGO-based TFTs, three main strategies are typically employed: (i) optimization of preparation process, (ii) doping of the active layer, and (iii) post-deposition treatment of the thin film.

2.2.1 *Optimization of preparation process*

IGO thin films are typically deposited by Physical Vapor Deposition (PVD) techniques, such as sputtering and Pulsed Laser Deposition (PLD), which enable precise control over film thickness and composition to achieve the desired electrical and optical properties. Among these, sputtering has been widely employed to fabricate high-performance IGO TFTs. In 2012, Ebata et al. [22] first reported the use of Direct Current (DC) magnetron sputtering to prepare polycrystalline IGO channel layers, achieving a mobility of 39.1 cm^2 V^{-1} s^{-1} and demonstrating the strong potential of IGO TFTs for next-generation display backplanes. Subsequent efforts have focused on optimizing sputtering process parameters to further enhance device performance. Peng et al. [23] systematically optimized the growth temperature and film thickness of amorphous IGO active layers via magnetron sputtering. As the deposition temperature increased from 160 °C to 220 °C, the mobility improved from 15 to 35 cm^2 V^{-1} s^{-1}, while the root mean square surface roughness decreased from 1.21 nm to 0.41 nm. And Furuta et al. [24] prepared amorphous IGO: H thin films by H_2-doped Radio Frequency (RF) magnetron sputtering, achieving a maximum field-effect mobility of 50.6 cm^2 V^{-1} s^{-1}.

Oxygen Partial Pressure (OPP) has a significant impact on the properties of In_2O_3-Ga_2O_3 films targeted for TFTs applications. Gonçalves et al. [25] reported that IGO films deposited under oxygen-free conditions exhibit a polycrystalline structure, whereas those prepared under an oxygen-containing atmosphere are amorphous. By varying the OPP value by an order of magnitude, the resistivity of IGO TFTs can be controlled over a wide range from 1.8×10^{-3} to 10^4 Ω·cm. Subsequently, Bak et al. [26] further revealed that adjusting the OPP during magnetron sputtering enables a trade-off between high mobility and device stability. These studies collectively indicate that optimizing the film composition and deposition parameters is an effective route to enhance device performance. For instance, Guo et al. [27] proposed a liquid InGa alloy printing approach to fabricate sub-5 nm ultrathin IGO films, demonstrating that the Ga_2O_3 content can be precisely tailored across the full compositional range, which dramatically reduces the turn-off current and enhances the device's resistance to ultraviolet interference. In addition to OPP, the deposition power also affects the concentration of oxygen vacancies, which act as charge carriers. Although oxygen vacancies are primarily governed by the indium content, increasing the sputtering power of the In_2O_3 target can generate more oxygen vacancies, thereby improving device performance. Moreover, IGO TFTs have also been explored for photodetector applications, leveraging their photo-sensitive properties [28].

Beyond sputtering, Atomic Layer Deposition (ALD) has emerged as an alternative technique for fabricating high-quality IGO channels. In 2020, Yang et al. [29] investigated the influence of gallium concentration on the structural evolution of ALD-grown IGO ($In_{1-x}Ga_xO$) thin films. They found that the $In_{0.66}Ga_{0.34}O$ composition exhibits fewer grain boundaries, higher mass density, and lower oxygen-vacancy defect density, resulting in the most stable behavior under external gate bias, as shown in Figure 3 and Table I. Zhang et al. [30] further advanced ALD-based IGO TFTs by fabricating ultrathin (∼ 3 nm) channels at a low temperature of 250 °C. The devices maintained excellent switching characteristics even at a channel length of 80 nm, with an I_{on}/I_{off} of $\sim 1.8 \times 10^{10}$ and a subthreshold swing of ∼ 92 mV dec^{-1}, demonstrating robust suppression of short-channel effects. This work represents the first demonstration of high-performance IGO TFTs with sub-100 nm dimensions, highlighting their potential for Back-End-of-Line (BEOL)-compatible monolithic 3D integration . More recently, a highly ordered and thermally stable crystalline IGO film was obtained by ALD using a novel gallium precursor, rendering the IGO film promising as a channel material in next-generation three-dimensional memory devices [31].

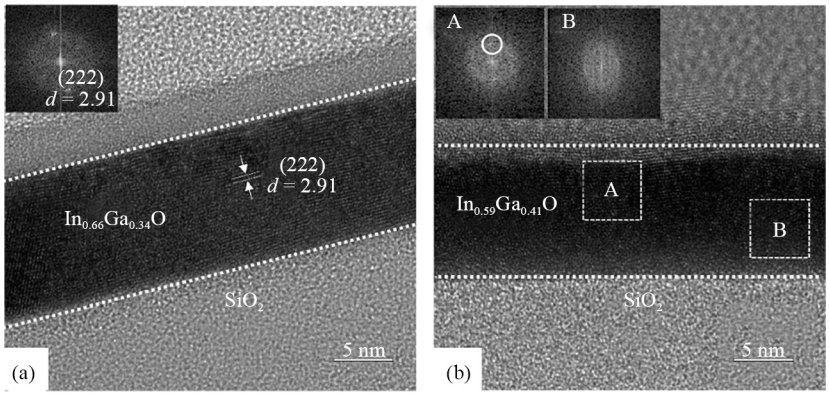


Figure 3. Cross-sectional HR-TEM image of (a) $In_{0.66}Ga_{0.34}O$ and (b) $In_{0.59}Ga_{0.41}O$ films at $T_A = 700$ °C on the SiO_2/Si substrate. Diffraction patterns obtained from a Fast Fourier Transform (FFT) were inserted in the inset of each image [29]

Table 1. Variations in the vertical grain size and lattice constant for the IGO films with different Ga concentrations at $T_A = 400$ and 700 °C [29]

ID	T_A (°C)	$In_{0.82}Ga_{0.25}O$	$In_{0.75}Ga_{0.25}O$	$In_{0.66}Ga_{0.34}O$	$In_{0.59}Ga_{0.41}O$
Vertical grain size (nm)	400	12	11		
	700	12.4	11.9	12.7	
Lattice constant (A)	400	10.02 ± 0.02	10.00 ± 0.01		
	700	10.04 ± 0.01	10.01 ± 0.01	9.94 ± 0.01	

Separately, Rabbi et al. [32] reported the preparation of high-performance coplanar amorphous $In_{0.5}Ga_{0.5}O$ TFTs by Spray Pyrolysis (SP) deposition on Polyimide (PI) substrates. The SP a-IGO films deposited at 370 °C contained less than 8% nanocrystalline In_2O_3 dots and exhibited a mass density of 6.6 g cm^{-3}. The resulting a-IGO TFTs on PI showed excellent performance in terms of threshold voltage, linear field-effect mobility, and subthreshold swing. Collectively, these studies—spanning different deposition techniques (sputtering, ALD, and spray pyrolysis) and process parameters (oxygen partial pressure, deposition power, temperature, and film thickness)—have successfully enhanced the mobility, stability, and overall electrical performance of IGO thin films, providing valuable insights for further optimization of IGO-based TFTs.

2.2.2 *Doping of the active layer*

Doping is a widely adopted strategy in semiconductor technology to tailor the electrical, optical, and magnetic properties of materials by introducing external atoms or molecules that modify the chemical composition or lattice structure [5]. Doping can be achieved through various techniques, this section reviews recent advances in doping strategies for IGO TFTs.

Nitrogen doping has been extensively investigated for its ability to passivate oxygen vacancies and enhance device stability. In 2019, Cheng et al. [33] introduced nitrogen during channel deposition and found that an appropriate nitrogen flow rate significantly reduces oxygen vacancies and improves the stability of IGO TFTs under positive gate bias stress, as shown in Figure 4. Furthermore, nitrogen-doped IGO TFTs exhibit good photoresponsivity and enhanced wavelength selectivity, attributed to a reduced effective band gap that facilitates electron transitions and ultraviolet responsiveness, making them suitable for high-performance ultraviolet detectors [33]-[36]. Hydrogen doping has also emerged as an effective means to improve carrier transport. By adding Polyvinyl Alcohol (PVA) to aqueous precursor solutions, optimal H doping can be achieved, accompanied by a coordination transition of Ga from six-fold to four-fold. This configuration suppresses deep trap defect localization and reduces polyhedral distortion in the metal-oxide network, thereby enhancing

electron mobility [37]. This approach provides a viable pathway for efficient H doping in green-solvent-processed oxide films, holding promise for high-performance and ultra-stable metal-oxide semiconductor devices.

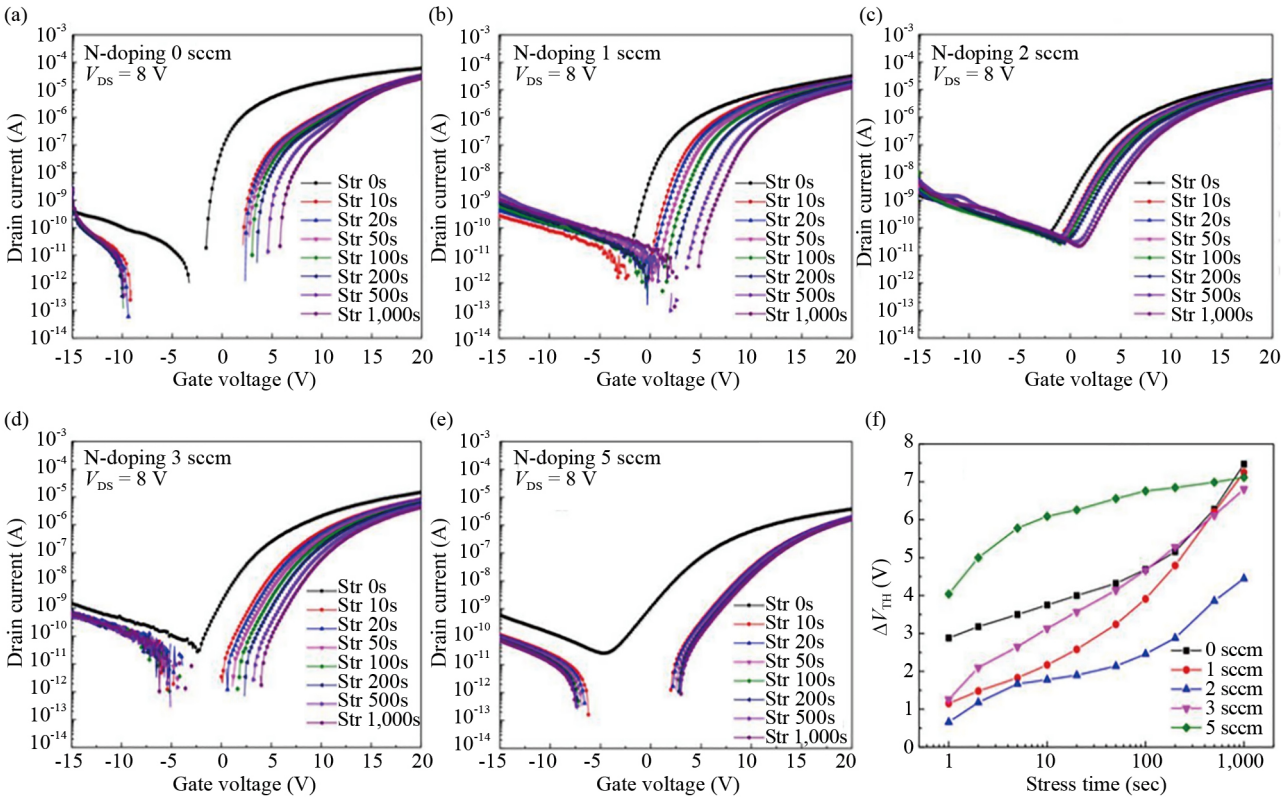


Figure 4. I-V hysteresis transfer characteristics measured from IGO TFTs with nitrogen ratio of (a) 0, (b) 1, (c) 2, (d) 3 and (e) 5 sccm [33]

In 2021, Zhu et al. [38] studied Praseodymium doped Indium Gallium Oxide (PrIGO) TFTs and found that the low-frequency noise of PrIGO-TFT devices mainly comes from the channel region, rather than the source/drain contact region. This finding offers a new perspective for mitigating light-induced negative bias instability caused by oxygen vacancies in oxide TFTs. In 2020, Kao et al. [39] incorporated titanium into IGO films, which increased the film capacitance and enhanced the pH sensitivity to 60.8 mV/pH, demonstrating potential for sensing applications. Meanwhile, Kang et al. [40] doped germanium into ITO thin films, achieving improved surface morphology and higher mobility compared to conventional ITO electrodes, suggesting a promising direction for future IGO TFT optimization. More recently, Bae et al. [41] directly grew crystalline lanthanum-doped InGaO (LaInGaO) thin films by spray pyrolysis at a substrate temperature of 375 °C, and systematically investigated the effects of La doping ratio (0%-20%) on film structure, defect states, and TFT performance. X-ray Photoelectron Spectroscopy (XPS) analysis revealed that the introduction of La effectively suppressed oxygen vacancies, benefiting from the high La-O bond dissociation energy. At an optimal La doping ratio of 7%, the devices achieved the best overall performance, with a threshold voltage of $\sim$ 0.01 V, mobility of $\sim$ 30.63 cm^2 V^{-1} s^{-1}, and subthreshold swing of $\sim$ 0.23 V dec^{-1}. This work demonstrates that appropriate La doping can effectively suppress oxygen vacancies in high-In-content IGO, serving as an effective active-layer doping strategy to tune threshold voltage and enhance device stability.

Doped thin film technology provides important ideas for the optimization of future IGO TFTs by introducing external atoms or molecules to change the chemical composition or lattice structure of the material. These reported doping strategies—encompassing both non-metal (N, H) and metal (Pr, Ti, Ge, La) dopants—provide diverse pathways for optimizing the performance of IGO TFTs, with demonstrated potential for applications in electronic devices and sensors.

2.2.3 *Post-deposition treatment of the thin film*

Post-deposition treatment is typically employed to repair as-deposited films and activate the rearrangement of internal atoms, thereby achieving a more ordered film structure and improved electrical properties. Recent advances in IGO TFTs have demonstrated that various post-treatment strategies—including annealing atmosphere engineering, non-equilibrium thermal processing, and crystallization time optimization—can significantly enhance device performance.

In 2022, Hong et al. [16] reported that polycrystalline IGO TFTs with a coplanar structure can be obtained by N_2O annealing. The resulting devices exhibited very stable environmental stability even after storage under high humidity and elevated temperature for two days, demonstrating the effectiveness of N_2O treatment in passivating defects and enhancing reliability. In 2025, To address the inherent trade-off between threshold voltage and mobility in amorphous oxide semiconductors, Ye et al. [42] proposed a localized ozone passivation technique. Using ALD-grown InGaO dual-gate TFTs, they applied a short-time O_3 treatment exclusively to the channel region, effectively reducing oxygen vacancies. This resulted in a positive shift of V_{th} to 0.15 V while maintaining a high mobility of 52 cm^2 V^{-1} s^{-1}, demonstrating that O_3 treatment can significantly improve channel interface quality without compromising carrier concentration in the contact regions. In a related study, Yang et al. [43] applied O_3 post-treatment to ALD-grown ultrathin IGO TFTs. O_3 effectively passivated oxygen vacancies, transforming high-In-content (90%) devices from non-switchable to high-performance operation, with an SS of $\sim$ 65 mV dec^{-1} and a mobility of 47.1 cm^2 V^{-1} s^{-1}.

In 2025, Zhang et al. [44] proposed a novel non-equilibrium annealing method, Nitrogen-Spike Annealing (NSA), for post-crystallization treatment of IGO films. This approach employs multiple transient high-temperature spikes (peak $\sim$ 490 °C, $\sim$ 27 s per spike) to induce crystallization while maintaining the overall thermal budget equivalent to conventional annealing at 400 °C. X-Ray Diffraction (XRD) and Electron Backscatter Diffraction (EBSD) characterization revealed that NSA-treated IGO films exhibit a more concentrated grain-size distribution and a superior (222) preferred orientation. Benefiting from the improved crystallinity and the stabilization of oxygen by Ga-O bonds, the NSA-treated IGO TFTs achieved a mobility of $\sim$ 86.2 cm^2 V^{-1} s^{-1} and a threshold voltage shift of only $\sim$ 6 mV under 2000 s of positive bias stress. This work demonstrates the potential of non-equilibrium annealing for realizing high-performance IGO TFTs under a BEOL-compatible thermal budget.

In the study of post-annealing treatment for InGaO (IGO) active layers, Rabbi et al. [45] systematically investigated the effect of Crystallization Time (t_{cr}) at 450 °C on film structure and device performance. IGO TFTs with short-time crystallization (3 min) exhibited a low subthreshold swing (SS $\sim$ 172 mV dec^{-1}) and moderate mobility, whereas extending t_{cr} to 60 min resulted in a fully nanocrystalline film with increased density (6.81 g cm^{-3}) and significantly reduced oxygen vacancy and hydroxyl-related defects. The corresponding devices achieved an ultra-large SS ($\sim$ 1,396 mV dec^{-1}) and higher mobility ($\sim$ 61.8 cm^2 V^{-1} s^{-1}), along with excellent bias-stress stability ($\Delta V_{th} \approx \pm 0.15$ V). This work demonstrates that post-annealing crystallization time can independently tune both grain-boundary defect states and intrinsic defects in IGO, offering an effective process route for high-SS, high-stability IGO driving TFTs.

These post-deposition treatment strategies—encompassing annealing atmosphere engineering (N_2O, O_3), non-equilibrium thermal processing (NSA), and crystallization time optimization—provide versatile and effective routes for repairing film defects, activating atomic rearrangement, and achieving high-performance IGO TFTs with enhanced mobility, stability, and switching characteristics. Future efforts may focus on further refining annealing process parameters or exploring alternative post-treatment methods to unlock additional performance gains.

2.3 *Gate dielectric engineering*

The gate dielectric is a critical component in TFTs, governing gate-to-channel capacitive coupling and directly influencing operating voltage, subthreshold swing, and overall device performance. Optimization of the gate dielectric for IGO TFTs primarily encompasses material selection, thickness adjustment, structural design, doping engineering, and process refinement.

Historically, SiO_2 has been the most commonly used gate dielectric since the advent of transistors. However, as device dimensions continue to scale down, ultra-thin SiO_2 layers suffer from severe quantum tunneling-induced leakage currents, which degrade device operation and may even lead to dielectric breakdown under high electric fields [46]. To

overcome these limitations, high-permittivity (high-*k*) dielectric materials have been introduced as gate insulators for IGO TFTs, offering enhanced gate control and reduced leakage. Notably, the incorporation of Al_2O_3 as a high-*k* gate insulator effectively reduces the operating voltage and subthreshold swing of IGO TFTs. In 2020, Chen et al. [47] demonstrated that ALD-deposited Al_2O_3 gate dielectric significantly reduces interface trap density in IGO TFTs, achieving an I_{on}/I_{off} ratio of 7.39×10^7, a subthreshold swing of 0.096 V dec^{-1}, and a field-effect mobility of 5.36 cm^2 V^{-1} s^{-1}. In the same year, Kim et al. [48] employed a high-*k* ion-gel film as the dielectric layer and found that the transistor can independently control two channels formed by the top and bottom gate dielectrics, achieving high mobility and excellent operational stability.

As a compelling example of high-*k* dielectric engineering for high-voltage applications. Hao et al. [49] reported IGO high-voltage TFTs featuring an Al-doped HfO_2 gate insulator grown by atomic layer deposition. Owing to the excellent gate control afforded by the high-*k* dielectric, the devices exhibited a breakdown voltage as high as 635 V and a mobility of 35 cm^2 V^{-1} s^{-1}, highlighting the considerable promise of high-*k* gate dielectric engineering in high-voltage scenarios. More recently, Choi et al. [50] demonstrated that the insertion of a SiO_2 interlayer between the HfO_2 gate dielectric and the IGO channel effectively eliminates remote Coulomb scattering, enabling high-mobility transport in ALD-grown IGO TFTs. This interlayer engineering approach further expands the design space for high-performance gate stacks.

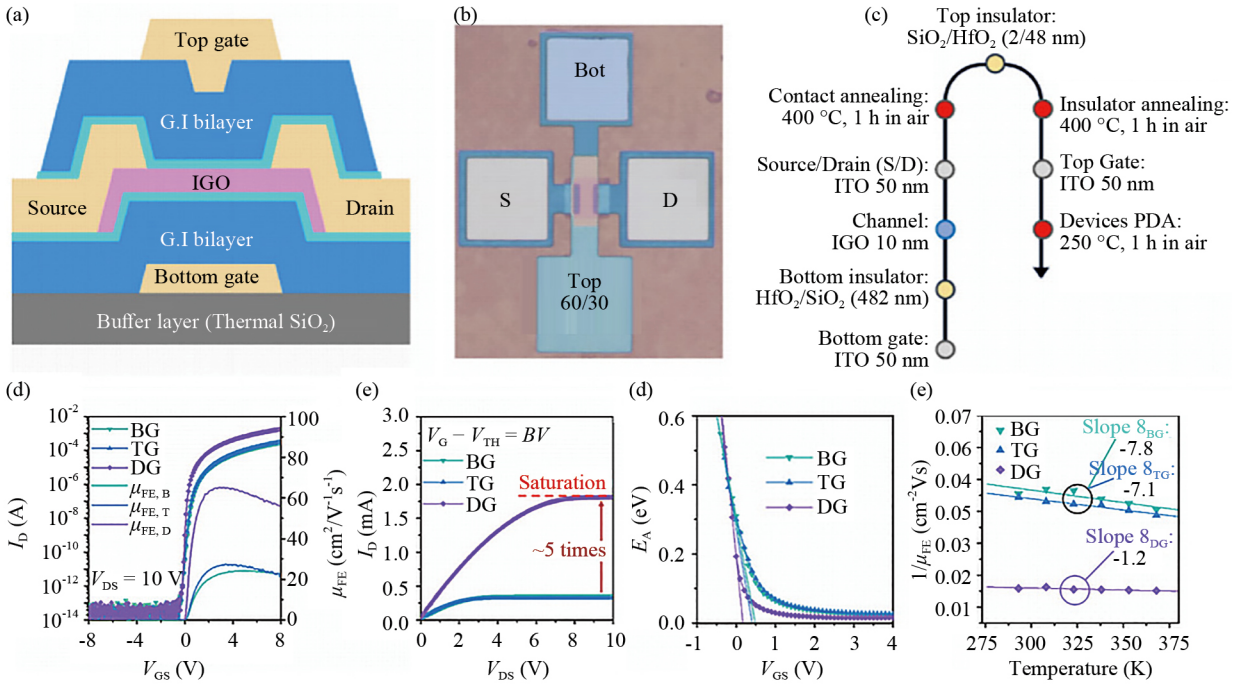


Figure 5. (a) A cross-sectional schematic of a DG IGO TFTs; (b) A false colored top view image; (c) The device fabrication procedure; (d) transfer characteristics at VDS = 10 V; (e) output characteristics; (f) variation of EA; and (g) $1/\mu_{FE}$-T characteristics [50]

Beyond material selection, gate structural design exerts a profound influence on device performance. Optimizing the gate architecture can improve electric field distribution, reduce charge accumulation, and thereby enhance device speed and efficiency [51]. In 2024, Choi et al. [50] researched high-performance IGO TFTs with a Double-Gate (DG) structure was developed using ALD. The fabricated DG TFTs exhibit outstanding device performances with μ_{FE} of 65.1 ± 2.3 cm^2 V^{-1} s^{-1}, subthreshold swing of 65 ± 1 mV dec^{-1}, and V_{th} of 0.42 ± 0.05 V, as shown in Figure 5. In 2025, Sun et al. [52] demonstrated a dual-gate amorphous IGO TFT operated in dual-sweep mode, where both top and bottom gates are simultaneously biased. Unlike conventional single-gate operation, the dual-gate dual-sweep configuration induces a bulk accumulation effect, enabling charge transport throughout the entire thickness of the active layer rather than solely at the

gate insulator interface. This work highlights that dual-gate architecture is an effective gate-engineering strategy to boost drain current without sacrificing stability, making a-IGO TFTs competitive with p-type LTPS for AMOLED backplanes.

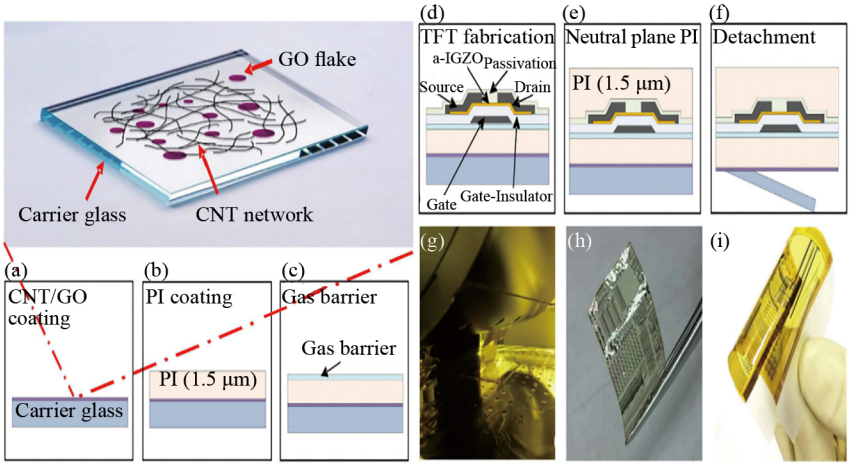


Figure 6. Fabrication process flow of neutral plane TFTs on a 1.5 μm PI substrate [53]

Significant advancements in gate dielectric engineering have been achieved through the adoption of high-*k* dielectric materials, dual-gate structures, and optimized deposition and patterning processes. The emergence of interlayer engineering (e.g., SiO_2 insertion in HfO_2 gate stacks) and the continued refinement of dual-gate architectures further expand the performance envelope of IGO TFT. However, precise control of gate process parameters and thickness tuning remain technically challenging and warrant further investigation. Besides, an excellent substrate can also improve the stability of TFT devices, as illustrated in Figure 6. Kim et al. [53] demonstrated a highly robust neutral-plane oxide TFT architecture that achieves exceptional mechanical stability by fabricating devices on an ultrathin (1.5 μm) Polyimide (PI) substrate and encapsulating them with a top PI film of equal thickness. Looking forward, greater attention may be directed toward plastic substrates for flexible electronics applications.

2.4 *Contact engineering*

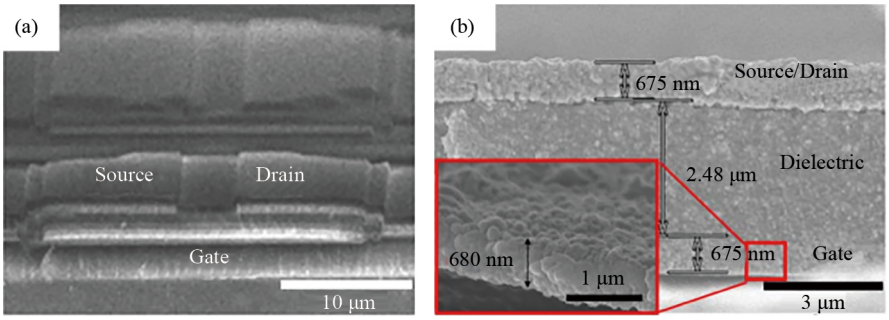


Figure 7. Basic structure of a bottom-gate Thin Film Transistor (TFT) using photolithography with (a) vacuum deposition and (b) all printed processes. Cross-sectional SEM image of an all printed TFT shows nonuniform structures at the interfaces between printed layers [54]

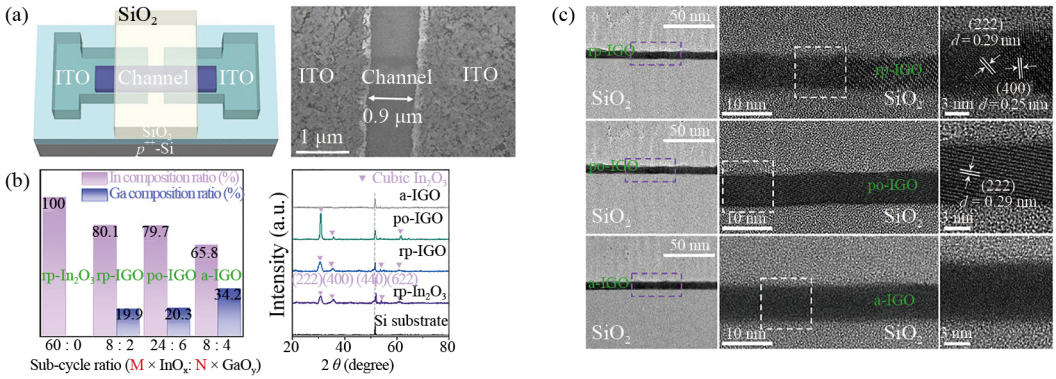
The interface between Source/Drain (S/D) electrodes and the semiconductor channel critically governs the electrical performance of oxide Thin-Film Transistors (TFTs), as it directly determines contact resistance, threshold voltage stability, and overall device reliability, as shown in Figure 7 [54]. In scaled devices, the influence of contact resistance becomes particularly pronounced, with oxide semiconductor TFTs typically exhibiting contact resistance four orders of magnitude

higher than that of conventional silicon MOSFETs [55]. Consequently, contact engineering has emerged as a vital research frontier for IGO TFTs. Recent advances in this area encompass electrode material selection, stacked electrode design, interlayer insertion, and wet chemical treatment, each offering distinct pathways to reduce contact resistance and enhance device performance.

The choice of S/D electrode material fundamentally determines the metal-semiconductor contact characteristics. Hu et al. [56] systematically investigated three metal electrodes (Ti, Cu, and Al) interfaced with ALD-grown 7 nm ultrathin IGO channels, revealing that contact behavior is predominantly governed by the reaction pathway and reversibility of interfacial oxygen redox chemistry rather than by work-function matching alone. Beyond single-layer electrodes, stacked metal structures offer additional degrees of freedom for contact optimization. Ye et al. [57] re-evaluated the impact of stacked electrodes (In/X, where X = Ag, Au, Cu, or Al) on a-IGO TFT performance and demonstrated that the top metal layer plays a significant role by modulating the effective work function of the stacked electrode. Some contact optimization strategies implemented in other oxide thin-film transistors may also provide valuable references for the future development of IGO TFTs. Jeong et al. [55] introduced a TiN/IGTO (3/8 nm) heterogeneous interlayer between S/D electrodes and the channel, achieving a specific contact resistivity of 9.0×10^{-6} $\Omega \cdot cm^2$ and improving mobility from 39.9 to 45.0 cm^2 V^{-1} s^{-1}; this multi-stack interlayer approach holds considerable promise for extension to IGO-based systems. In the field of printed electronics, Liang et al. [58] took an unconventional approach by actively exploiting the coffee-ring effect: the ultrathin central region of the printed film serves as the high-mobility channel, while the thicker edge regions are directly employed as S/D electrodes, enabling fully inkjet-printed ITO transistors with a saturation mobility of 34.9 cm^2 V^{-1} s^{-1}.

Among the various contact engineering strategies, Kim et al. [59] provided a mechanistic understanding of contact region reliability through crystallographic orientation engineering. They demonstrated that preferentially (222)-oriented IGO (po-IGO) thin films, deposited by Atomic Layer Deposition (ALD), effectively suppress the lateral diffusion of oxygen vacancies from the source/drain junction into the channel along grain boundaries. In conventional randomly oriented polycrystalline IGO (rp-IGO), grain boundaries serve as fast diffusion paths for oxygen vacancies, shortening the effective channel length (L_{eff}) and inducing severe Drain-Induced Barrier Lowering (DIBL). The po-IGO architecture mitigates this issue by reducing grain boundary density and blocking lateral vacancy migration, thereby preserving a longer L_{eff} even at the same patterned dimension. The crystallographic-structure-dependent L_{eff} variation was further corroborated by Technology Computer-Aided Design (TCAD) simulations. This work fundamentally elevates contact optimization from conventional electrode/interface engineering to the realm of semiconductor channel crystallographic engineering, offering a new paradigm for suppressing short-channel effects in future highly scaled oxide TFTs (Figure 8) [59].

The above studies indicate that optimizing the Source/Drain (S/D) contact region—whether through structural design or material engineering—is an effective approach to enhancing the performance of IGO-based TFTs. These findings regarding the source/drain may offer new insights for subsequent optimization efforts.



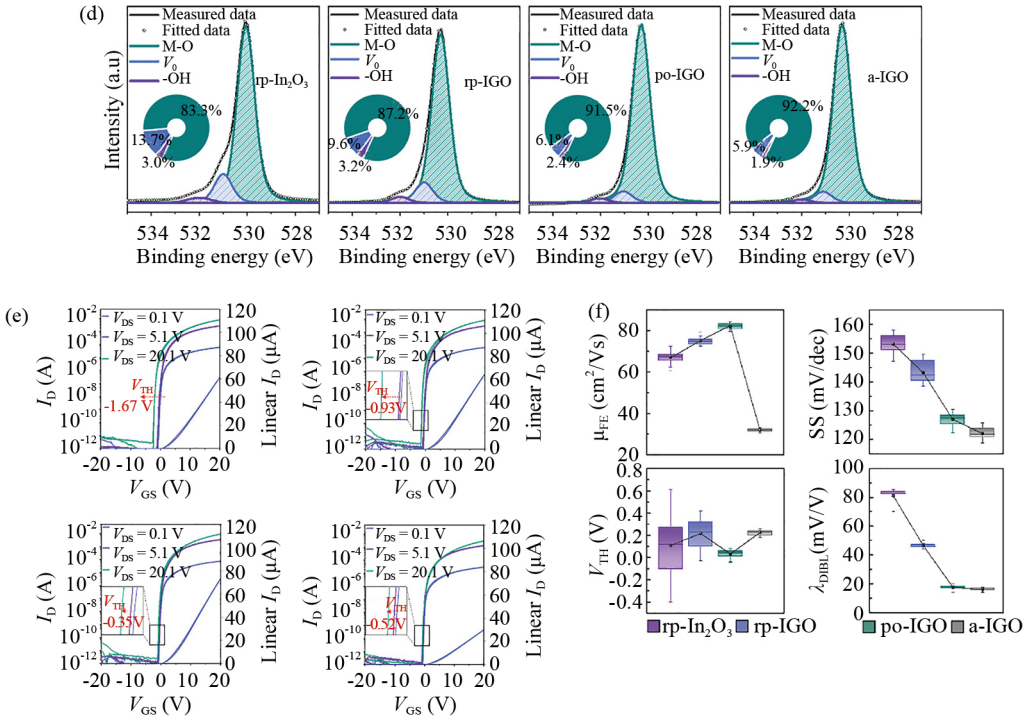


Figure 8. (a) Schematic of a fabricated TFT and the top view SEM image of a 0.9μm long TFT. (b) Cation composition ratios confirmed through XRF and The GIXRD patterns. (c) Cross-sectional HR-TEM images of the fabricated thin-films: rp-IGO, po-IGO and a-IGO. (d) O 1s spectra of the fabricated thin-films: rp-In_2O_3, rp-IGO, po-IGO and a-IGO. (e) Transfer characteristics of the fabricated 0.9 μm long TFTs: rp-In_2O_3, rp-IGO, po-IGO and a-IGO. (f) Electrical figures of merit of the fabricated 0.9 μm long TFTs: μ_{FE}, SS, V_{TH} and λ_{DIBL} (data taken from 15 devices per condition) [59]

2.5 *Interface engineering*

Interface optimization in IGO TFTs primarily involves the modification of the active layer and related interfacial structures to improve device performance, stability, and reliability. The density of trap states in oxide TFTs is highly susceptible to the adsorption of ambient species—particularly water and oxygen—on the top channel surface, and H_2O adsorption on the back-channel surface can severely degrade electrical properties [5]. Consequently, passivation layers and interfacial engineering have become critical strategies for enhancing IGO TFT performance.

The passivation layer has attracted considerable attention as a means to protect the channel from environmental degradation and reduce interface trap density. In 2025, Chen et al. [60] designed and successfully realized a sandwich-encap-sulation structure for high-performance, hysteresis-free a-IGO TFTs using magnetron-sputtering-prepared IGO films encapsulated with ALD-grown Al_2O_3 bilayers (Figure 9). Remarkably, the devices achieved an exceptionally low hysteresis of merely 0.04 V, representing a significant improvement over conventional structures. Additionally, an environmentally friendly superhydrophobic composite layer—composed of bifunctional self-assembled nanoparticles combined with vinyl polyhedral oligomeric silsesquioxane—has been applied to IGO TFTs, demonstrating outstanding protection under harsh environmental conditions [61].

Beyond passivation, bilayer channel structures have emerged as an effective interface engineering strategy to simultaneously enhance mobility and stability. The concept of bilayer channel engineering for IGO-based TFTs was pioneered by Yu et al. [62], who demonstrated that In_2O_3/IGO double-layer TFTs achieve significantly higher mobility and superior on/off current ratios compared to single-layer IGO and In_2O_3 devices (Figure 10). In 2017, Yang et al. [63] first demonstrated that double-layer IGO films prepared by dual-target co-sputtering significantly outperform single-layer IGO films, achieving a mobility of 53.2 cm^2 V^{-1} s^{-1}, a subthreshold swing of 0.19 V dec^{-1}, and an I_{on}/I_{off} of $\sim 10^7$. In 2021, He et al. [64] fabricated In_2O_3/IGO heterojunction TFTs via a solution process using water as the solvent, achieving a carrier mobility approximately 14 times higher than that of single-layer IGO TFTs (Figure 11). In 2025, Wen et al. [65] prepared

stacked IGO/IGZO channel films consisting of an indium-rich IGO layer and a conventional IGZO layer using atomic layer deposition, the optimized structure promotes preferential growth of nanocrystalline IGZO with matched crystal orientation in the channel, facilitating electron transport. Gui et al. [66] reported a solution-processed heterojunction-channel IGO/AlInGaO (IGO/AIGO) TFTs. The large conduction band offset causes electron accumulation at the heterojunction interface, forming a quantum trap that cooperates with the main electron path to create a double conductive path. Jeong et al. [67] employed a crystalline $In_{0.7}Ga_{0.3}O$ seed layer to induce continuous grain growth in high-Ga-content IGO ($In_{0.5}Ga_{0.5}O$ and $In_{0.4}Ga_{0.6}O$) top layers, promoting crystallization and effectively suppressing oxygen vacancy formation; the resulting 0.3 μm-channel-length TFTs achieved a near-zero threshold voltage. In 2026, Xu et al. [68] proposed an IGO/IZTO heterogeneous stack to overcome the mobility-stability trade-off through band engineering. The front channel (adjacent to the gate insulator) consists of high-carrier-concentration IGO for efficient charge transport, while the back channel comprises wide-bandgap IZTO to suppress photoionization of oxygen vacancies under illumination. He et al. [69] fabricated bilayer IGO/IGZO TFTs by magnetron sputtering, inserting a highly conductive IGO thin film between the insulating layer and the IGZO layer. Based on the synergistic effects of defect self-compensation and bandgap engineering, the bilayer devices achieved a mobility improvement from 20.5 to 51.6 $cm^2 V^{-1} s^{-1}$, providing a simple pathway for low-cost manufacturing of high-performance oxide TFTs.

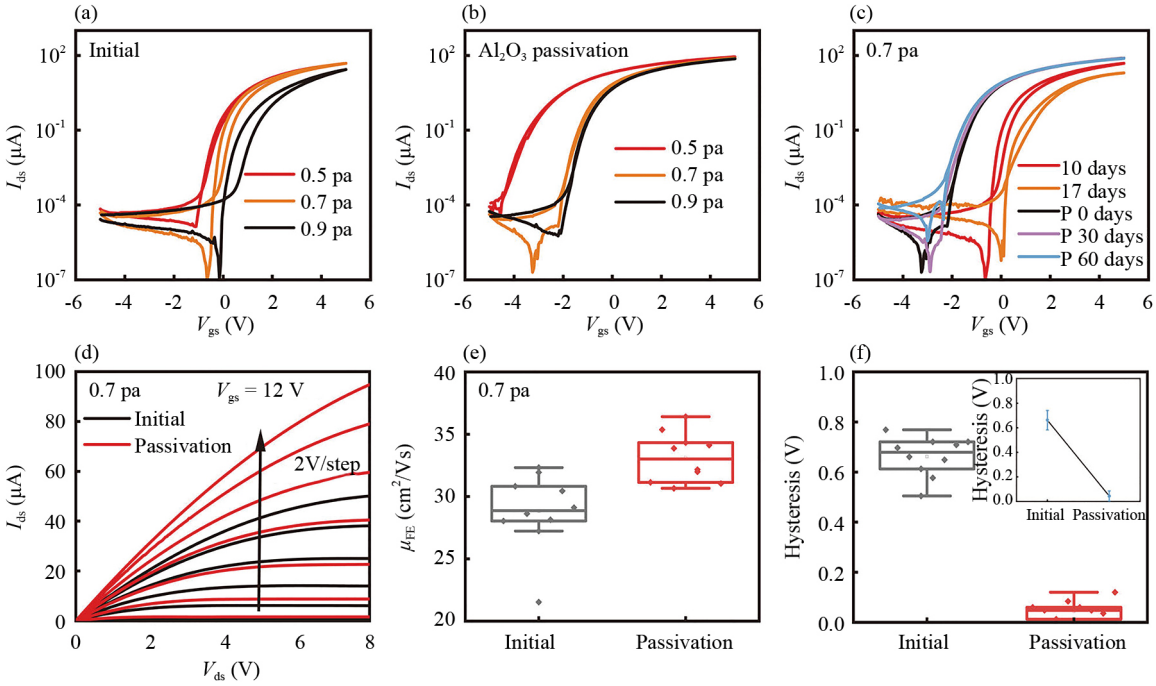


Figure 9. (a) and (b) Transfer characteristic curves of the initial device and the passivated device prepared under different pressures, respectively. (c) Transfer characteristic curve of the device prepared at 0.7-Pa pressure after being exposed to air for two months. Note that, "T" represents the initial device and "P" represents the passivated device. (d)-(f) Output characteristic curves (d) of the initial device and the passivated device prepared at 0.7-Pa pressure, statistics of μ (e) and hysteresis (f) of ten initial devices and passivated devices [70]

Collectively, these interface engineering strategies—encompassing passivation layer encapsulation and bilayer/heterojunction channel design—have proven effective in reducing interface trap density, suppressing hysteresis, and simultaneously enhancing mobility and bias stability. These approaches offer versatile pathways for achieving high-performance, reliable IGO TFTs suitable for next-generation display applications.

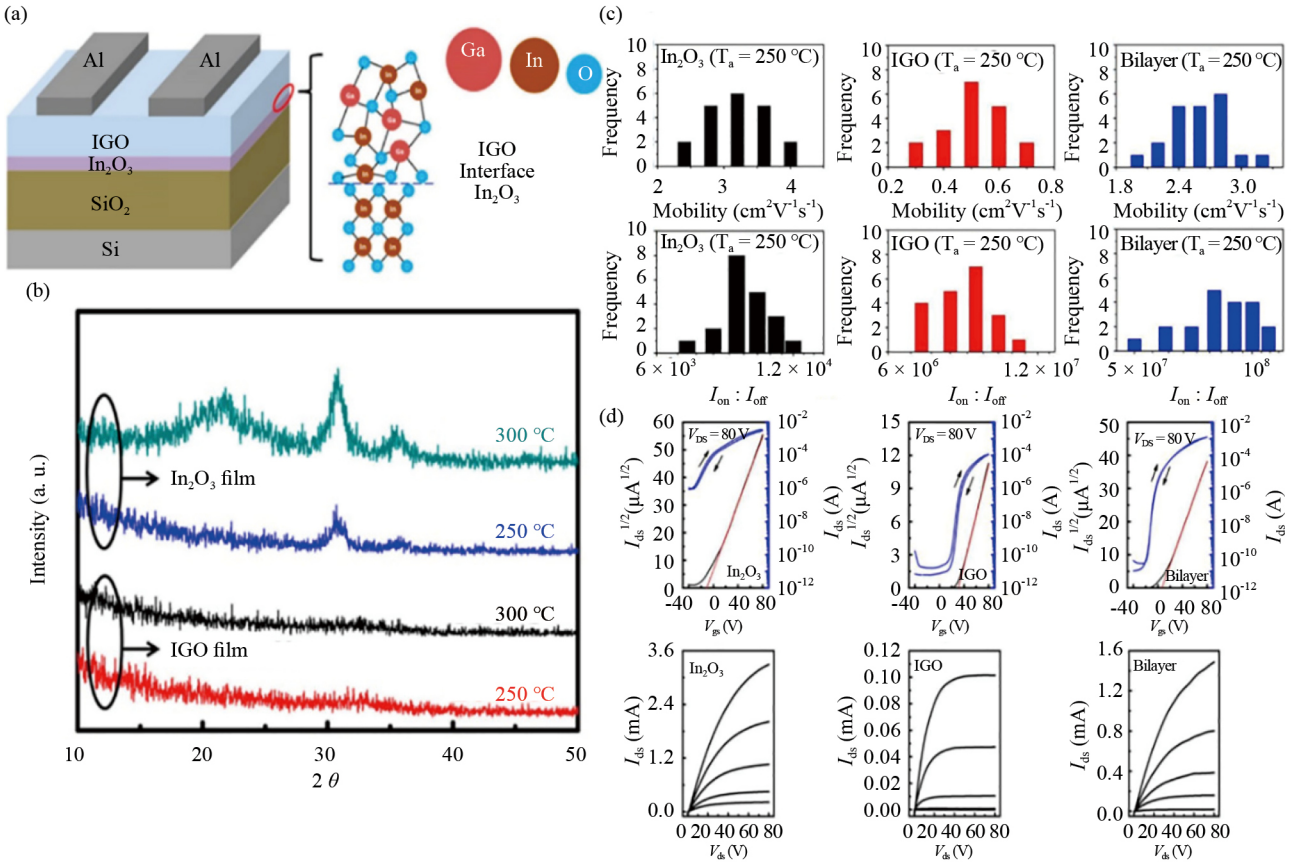


Figure 10. (a) In_2O_3/IGO bMO TFT device architecture employed in this study and schematic representation of a metal oxide lattice. (b) θ-2θ XRD scans of 15 nm In_2O_3 and IGO films deposited on SiO_2 substrates and annealed at the indicated temperatures. (c) Saturation TFT mobility and current I_{on}/I_{off} plots for single layer In_2O_3 TFTs, single layer IGO TFTs, and bilayer In_2O_3 (3 nm)/IGO (10 nm) TFTs, processed at 250 °C. (d) Typical transfer (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) plots of the indicated TFT devices: single-layer In_2O_3 TFT, single-layer IGO TFTs, and bilayer In_2O_3 (3 nm)/IGO (10 nm) TFT annealed at T = 250 °C [62]

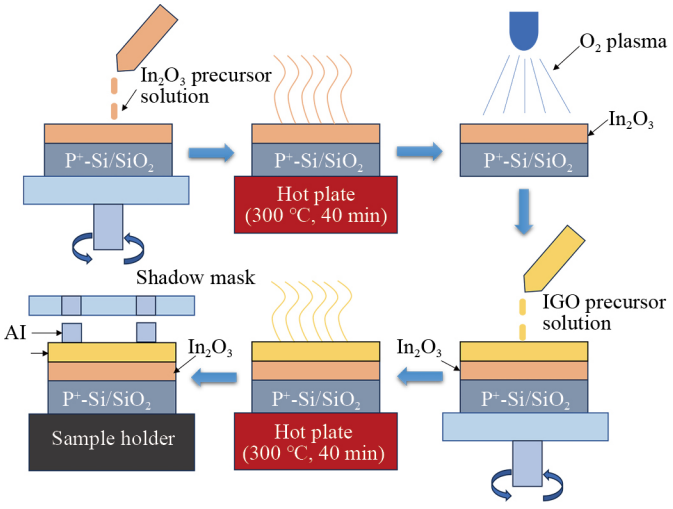


Figure 11. The fabrication process of the In_2O_3/IGO heterojunction transistor

2.6 *Device structure optimization*

Beyond material and interface engineering, device architecture design and geometric layout exert a profound influence on the electrical performance of IGO TFTs. Recent advances in structural innovations—including offset-region engineering, active-layer patterning, and field-plate architectures—have reshaped electric field distribution, carrier transport pathways, and breakdown characteristics, thereby addressing critical challenges such as short-channel effect suppression, high-voltage operation, and mechanical flexibility.

In the realm of lateral device layout design, offset-region engineering and active-layer patterning have emerged as effective strategies for enhancing the performance of short-channel and flexible devices. Rabbi et al. [70] systematically investigated the effects of offset engineering on coplanar polycrystalline IGO TFTs with a channel length of approximately 1 μm. By varying the offset length (1-3 μm) and the N^+ doping concentration, they elucidated the modulation mechanism of offset-region resistance on the effective drain voltage and on-current. Reducing the sheet resistance of the N^+ offset region to 14.5 Ω/sq effectively eliminated the dependence on offset length. The optimized TFTs achieved a mobility of approximately 86 cm^2 V^{-1} s^{-1}, a threshold voltage of approximately + 1.5 V, and excellent bias stability with $\Delta V_{th} \approx \pm 0.3$ V. For high-voltage applications, Hao et al. [71] proposed a selective F-plasma treatment strategy specifically for the offset region in top-gate high-voltage IGO TFTs. XPS analysis revealed that F-plasma treatment increased the oxygen vacancy concentration in the offset IGO film from 29.4% to 37.7%, thereby reducing the offset-region sheet resistance by 58.3%. Since the treatment was confined exclusively to the offset region, the channel region's threshold voltage (−2.2 V) and subthreshold swing (81 mV dec^{-1}) were preserved.

Active-layer patterning has emerged as a novel approach to enhance crystallinity and device performance. Moon et al. [72] patterned the amorphous IGO active layer into 1 μm-wide parallel strips on flexible polyimide substrates. During 450 °C annealing, the strip edges induced preferential nucleation and grain growth along the (222) orientation. The active-split TFT achieved a saturation mobility of 108.8 cm^2 V^{-1} s^{-1} and a threshold voltage of + 0.9 V, while maintaining stable performance after 10,000 folding cycles at a bending radius of 1 mm. Further systematic studies on glass substrates with unit widths ranging from 2 to 20 μm revealed that narrower unit widths increase the proportion of highly crystalline edge regions; 2-μm-wide devices achieved a mobility of 68.9 cm^2 V^{-1} s^{-1}, significantly higher than that of 20 μm-wide counterparts (43.2 cm^2 V^{-1} s^{-1}) [73].

For high-voltage applications, Qiu et al. [74] proposed a gate-field-plate structure for top-gate IGO TFTs. TCAD electrical simulations revealed that the field plate effectively shifts the peak electric field from the gate edge to the SiO_2 passivation layer, increasing the breakdown voltage from 547 V to 1,348 V—an improvement of approximately 2.4 times—while maintaining a low subthreshold swing of 95 mV dec^{-1} and a positive threshold voltage of 0.16 V. This work demonstrates that field-plate engineering is a highly effective strategy for overcoming the performance bottlenecks of high-voltage oxide TFTs.

In summary, recent advances in device structure optimization for IGO TFTs have provided practical solutions across multiple application domains. These architectural innovations, combined with the material, interface, and process optimizations discussed in preceding sections, collectively position IGO TFTs as a versatile platform capable of meeting the diverse demands of next-generation displays, high-voltage electronics, and flexible wearable devices.

3. Conclusion

Over the past two decades, substantial progress has been achieved in enhancing the performance of IGO TFTs through diverse process optimization strategies. This review systematically summarizes the major optimization approaches, with particular emphasis on active layer engineering—encompassing preparation process control, doping, and post-deposition treatment. In addition, we discuss recent advances in gate dielectric engineering, contact engineering, interface engineering, and device structure optimization. Across these five categories, the optimization of IGO TFT performance consistently converges on two core themes: rational material selection and precise tuning of fabrication processes. Furthermore, the incorporation of passivation layers and secondary materials has emerged as an effective complementary strategy to further enhance device reliability.

Despite the substantial improvements in field-effect mobility achieved through these strategies, device stability remains a critical challenge. A persistent trade-off between high mobility and good stability continues to hinder the practical deployment of IGO TFTs, and this issue must be systematically addressed as mobility benchmarks are progressively met. Achieving continuous mobility enhancement while simultaneously ensuring stability within acceptable limits will be an unavoidable focus for the future development of IGO TFTs. Although many challenges remain unresolved, IGO TFTs have already demonstrated clear advantages over conventional IGZO TFTs, particularly in terms of achievable mobility and compatibility with advanced fabrication techniques. Continued advancement of IGO TFT-related technologies—through synergistic optimization of materials, interfaces, and device architectures—will undoubtedly contribute to the realization of high-quality display panels and next-generation electronic devices in the future.

Author contributions

Z. L., C. S., J. Z. and D. L. were responsible for the general framework layout and task assignment, and participated in writing the main part of IGO TFTs. X. W. was responsible for writing the second part, and M. Y. was responsible for the image organization and format correction of the manuscript. H. H. was responsible for experiment conceptualization and project supervision. L. L. was responsible for manuscript revisions. All authors have approved the final version of the manuscript.

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Data availability

This study did not generate or analyze any new data. All information relevant to the study is available in the cited publications; therefore, data sharing is not applicable.

Conflict of interest

The authors declare no competing financial interest.

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