Journal of Electronics and Electrical Engineering
https://ojs.wiserpub.com/index.php/JEEE

UNIVERSAL WISER PUBLISHER

Research Article

In Depth Parasitic Capacitance Analysis on GaN-HEMTs with Recessed MIS Gate

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Received: 12 July 2022; **Revised:** 14 September 2022; **Accepted:** 15 September 2022; **Published:** 18 October 2022

Abstract: In this study, parasitic coupling capacitance behavior on GaN devices with recessed MIS (Metal-Insulator-Semiconductor)-gate is analysed in depth by combining experimental data, 2D-simulations, analytical calculations, and TEM (Transmission Electron Microscopy) imaging. This enabled to highlight the second channel formation. A new analytical model to determine the contribution of the active channel and the different coupling parasitic capacitances from a gate-to-channel capacitance C_{gc} curve of a GaN MIS-HEMT (Metal-Insulator-Semiconductor High Electron Mobility Transistor) is proposed. This also enables the evaluation of the respective contributions of all components such as the passivation layer and gate field plate capacitances in the parasitic capacitance and effective gate length evaluation of GaN devices with recessed MIS gate, which could be useful for reliable parameter extraction, device modeling and optimization.

Keywords: electrical characterization, modeling, power semiconductor devices, gate length, recess depth, normally-off, HEMT, GaN, 2D electron gas (2DEG), parasitic capacitance, 2D simulation

1. Introduction

Heterojunction device-based AlGaN/GaN High Electron Mobility Transistors (HEMTs) have attracted a lot of attention in power electronics and RF applications, which require high breakdown voltage and low ON-resistance [1–5]. With the fast development of GaN-based-device technology and circuit integration, reliable predictive models are of great value for circuit design and simulation [6]. The capacitance-voltage (C-V) characteristics, which are equally important for circuit simulation and modelling, have received less attention for GaN devices in the last decade. However, with the progressive miniaturization of these GaN devices for power electronics and RF circuit, different parasitic effects must be considered for a reliable device modelling and simulation [6–9]. For silicon technology, several methodologies have been proposed to analyse the parasitic components [10, 11], but this is less the case for GaN devices.

In previous studies [4, 12], gate-to-channel capacitance was measured and simulated for different gate lengths and recess depths. We proposed here a new methodology to extract the coupling parasitic components and effective gate length from gate-to-channel capacitance C_{gc} measurements. Zhang et al. [6] have reported the analytical modeling of

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capacitances for normally-On HEMTs, including parasitic components. However, few works have been dedicated to the effects of etching depth and device architecture on gate-to-channel coupling capacitance.

In this study, we present, for a first time, a new approach to analyse the C_{gc} characteristics of a GaN MIS-HEMT with recessed gate and to discriminate the active channel and parasitic capacitances. This will enable us to evaluate the electrical length of the active channel under the gate. We will first summarize the experimental details of this study, such as process technology, device architecture and electrical characterization protocol. Next, we will update a previous work on gate-to-channel capacitance measurements and 2D-simulation methodology of interest for this study [12]. We will also show the coupling capacitance variations and the formation of a second channel, observed in the simulated structure. All experimental and analytical methods, including various recess depths, have been validated with 2D simulations and were used to evaluate parasitic capacitances. Finally, we will compare the respective impact of parasitic channel length on C_{gc} capacitance and their influence on the extraction of the effective gate length of the active channel.

2. Device and experimental setup

We conducted the electrical measurements on two different wafers processed with normally-off GaN MIS-HEMT technology. GaN epitaxy (Figure 1a) was achieved by Metal-Organic-Chemical Vapor Deposition (MOCVD), on 200-mm diameter silicon (111) substrates [12]. The structure consisted of an AlN (Aluminum Nitride) nucleation layer, an AlGaN based buffer, C-doped GaN buffer layers to ensure a high breakdown voltage and of an unintentionally doped (UID) GaN channel in which a back-barrier could be inserted. The piezoelectric effect to form the 2D electron gas (2DEG) was obtained with the growth of AlN spacer and an $Al_xGa_{1-x}N$ barrier layer on top of the GaN channel layer, followed by in-situ deposition of a passivation layer [13, 14]. In this study, fully recessed Metal-Insulator Semiconductor (MIS) gate normally-off GaN devices were processed by dry etching of AlGaN and UID-GaN layers in the gate area. Figure 1b shows a cross sectional TEM of the fully recessed MIS gate region with different typical interfaces.

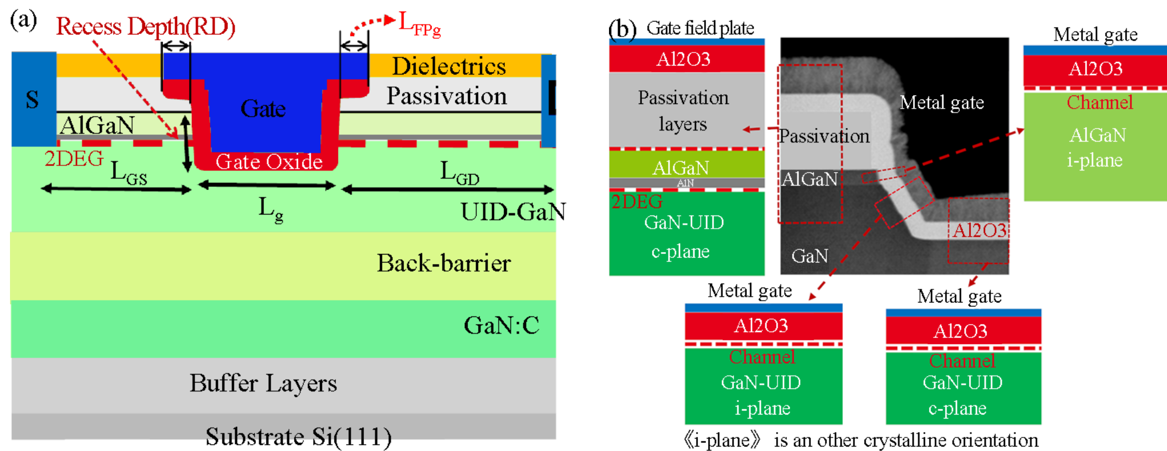

Figure 1. (a) Schematic cross section of GaN MIS-HEMT device with recess gate stack and (b) Cross-sectional TEM image of the recessed MIS gate region with different typical interfaces

The two studied wafers correspond respectively to two different recess depths, i.e., a shallow gate recess (RD1) and a deep gate recess (RD2). The gate recess was followed by the deposition of an oxide layer of Al_2O_3 by Atomic Layer Deposition and the metallic gate. The source and drain ohmic contacts were composed of Ti/AlCu metallic pads connected to the 2D electron gas (2DEG) formed at the AlGaN/GaN interface. The tested symmetrical T-gate devices have a gate field plate length of 0.25 µm (L_{FPg}) (Figure 1), 200 µm width (W) and channel lengths (L_g) ranging from 0.25 µm to 2 µm. The total gate-to-channel capacitance C_{gc} was measured with a HP 4284 LCR meter. The "High" entry of the LCR meter

was connected to the gate electrode with a 40 mV AC signal. The "Low" entry of the LCR meter was connected to the source and drain electrodes for the complex current measurement. The LCR-meter was calibrated using an open procedure in order to obtain the best accuracy for the capacitance measurements.

3. Gate-to-channel capacitance simulation results

3.1 *Methodology*

The capacitance C_{gc} (Equation (1)) was calculated using the total energy variation ΔW_e (Equation (2)) of the device for each increment of gate bias ΔV_g. It should be mentioned that this method was first used on FD-SOI (Fully Depleted Silicon-On-Insulator) device by Ben Akkez et al. [11] and was applied for the first time on AlGaN/GaN based devices in our previous work [12].

$$C_{gc}=\frac{2\Delta W_e}{\Delta V_g{}^2} \quad (1)$$

$$\Delta W_e = \int_{Device} \frac{\varepsilon \cdot \Delta E^2 + \Delta\rho \cdot \Delta V}{2} dv \quad (2)$$

where ΔE is the local electric field variation, ΔV the local potential change, $\Delta\rho$ the local charge density difference for gate bias varying from V_g to $V_g + \Delta V_g$ and $\varepsilon$the permittivity. The total energy variation is computed by integration of the electric field and space charge contributions over the device volume (Equation (2)) [11, 15]. It is worth noting that, in Equation (2), the local electric field term ($\varepsilon \cdot \Delta E^2/2$) prevails in dielectric-like regions with low charge density, whereas the local energy charge term ($\Delta\rho \cdot \Delta V/2$) dominates in accumulation/inversion regions when free carrier concentration increases [12].

3.2 *GaN MIS-HEMT devices simulation results*

The total gate-to-channel capacitance simulations have been carried out after solving the Poisson equation in a standard GaN MIS-HEMT device with recessed gate as shown in Figure 2. The simulated architectures were realized to match the TEM picture with different typical interface as those of Figure 1b. The GaN channel and AlGaN layers were taken as unintentionally doped (UID).

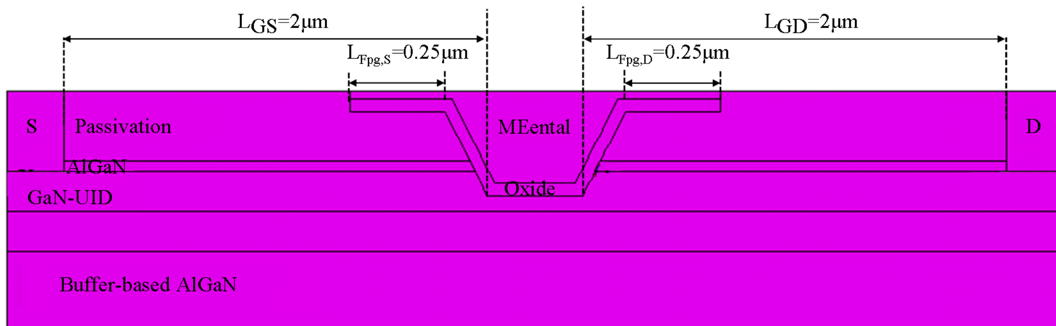

Figure 2. Schematic cross section of device used for the simulation

The parameters used for the simulation are: $\sigma_{GaN/AlGaN} = 0.9 \times 10^{13}$ cm^{-2}, $\sigma_{AlGaN/Passivation} = 0$ cm^{-2} and $C_{ox} = \varepsilon_{ox}/t_{ox} = 2.56 \times 10^{-7}$ F·cm^{-2} (for $t_{ox} \approx 30$ nm) [12]. The source and drain contact regions are electrically connected to the 2DEG, which is induced by the polarization charge at the AlGaN/GaN interface [16]. The electrons in the GaN and AlGaN layers are treated with classical Boltzmann statistics. The response of hole minority carriers is deactivated because it was not experimentally observed in these AlGaN/GaN devices. The source and drain ohmic contacts are grounded and the gate contact is DC biased to V_g.

To fit the lateral position of the experimental capacitance characteristics $C_{gc}(V_g)$ with simulation result, the flat-band voltage V_{fb} was adjusted. The total gate-to-channel capacitance (C_{gc}) was simulated for symmetrical GaN MIS-HEMT devices ($L_{GS} = L_{GD} = 2$ µm) with the parameters indicated previously. Figure 3a shows that good fits between experimental and simulation results can be achieved for different gate lengths. In Figure 3b are reported the maximum (at −4 V) and minimum (at 4 V) C_{gc} capacitances versus gate length for two different recess depths (RD1 and RD2). We can see the same minimum capacitance C_{gc} for $V_g = -4$ V and a linear dependence with L_g for $V_g = 4$ V. This confirms that the C_{gc} in depletion regime ($V_g \ll V_{fb}$) stems from the gate-to-2DEG coupling capacitance.

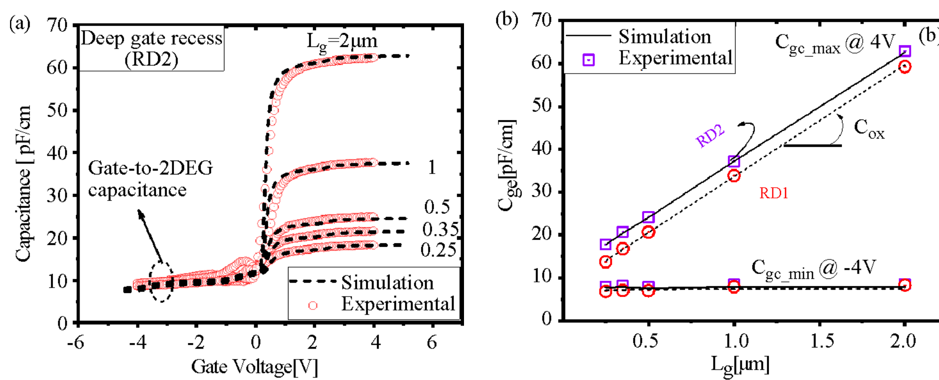

Figure 3. Experimental and simulation gate to-channel capacitance (a) C_{gc} versus V_g for different L_g for deep gate recess and (b) C_{gc} at $V_g = 4$ V and $V_g = -4$ V versus L_g for the two different wafers (deep and shallow gate recess)

Figure 4 shows a phenomenological result of the coupling capacitance simulation of a GaN device with recessed gate in the two operation regimes (depletion and accumulation). Figure 4a, b present the electron density profiles in accumulation and depletion regimes. We can see a particular shape of the source (or drain) electrode and its variation with gate voltage. As was explained in [12], we observe that, in depletion, the 2DEG region ends at a certain point P (Figure 4a) close to the oxide (Al_2O_3) interface. Therefore, the minimum capacitance C_{min} will come from the coupling between the source and drain contacts along the 2DEG located at the GaN/AlGaN interface up to its extremity at a certain point P and the gate contact. In accumulation regime, the 2DEG at source and drain sides are connected to the electron channel formed at the GaN/Al_2O_3 interface. However, we can see that a second channel appears along and above the AlGaN/Al_2O_3 interface as well as at the AlGaN/passivation interface (depending on gate bias, field plate length and polarization charge at this interface). Figure 4c, d show the potential profile and equivalent capacitance circuit for the different coupling areas in the gate region of a GaN HEMT device in depletion and accumulation regimes. The equipotential lines illustrate how the potential changes from source to gate contacts across the device. The electrostatic coupling is stronger in region where the potential drop is more abrupt. A coupling capacitance appears at negative gate bias due to the coupling between the horizontal source or drain electrodes formed by 2DEG and the gate electrode. Figure 4d shows that the coupling in accumulation stems from the coupling between the electron channel and the gate contact. The parasitic electron channel can extend along the AlGaN/Al_2O_3 interface farther than the effective channel L_{eff} (Figure 4b). These results agree with our previous results [12].

Moreover, a parasitic electrostatic coupling exists between the gate field plate and the electron channel at the AlGaN/passivation interface (Figure 4b). Therefore, a simulation study and an electrostatic coupling analysis above the 2DEG is necessary to evaluate the parasitic coupling capacitances, for further correction.

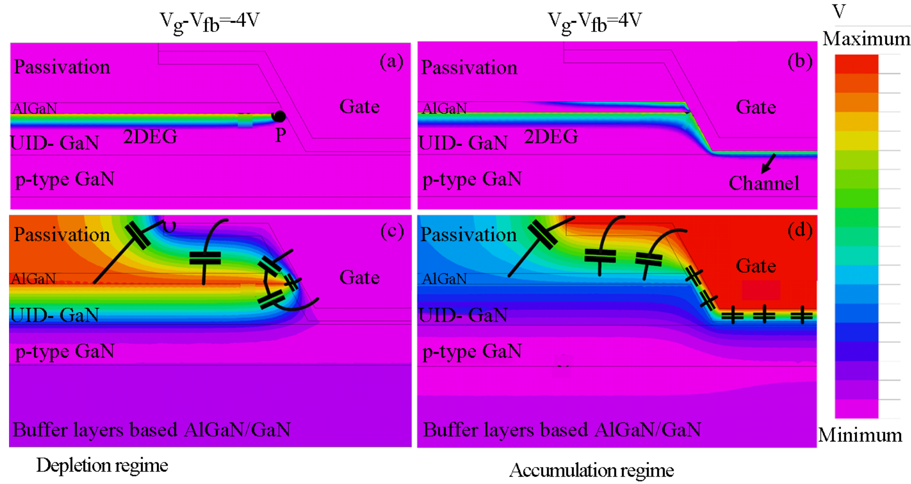

Figure 4. Map of half GaN MIS-HEMT device with recessed gate simulation illustrating (a, b) the electron density profile and (c, d) the potential profile in two operating regimes (depletion and accumulation)

3.3 *Dielectric behavior analysis of parasitic coupling*

As our main concerns are parasitic coupling capacitance C_{Par} and effective gate length L_{eff}, we will focus mainly on the analysis of parasitic capacitance in accumulation (Figure 4b, d). To simplify the simulation, the 2DEG has been replaced by a metal strip and the channel at Al_2O_3 interface or AlGaN/passivation interface by another metal strip (Figure 5).

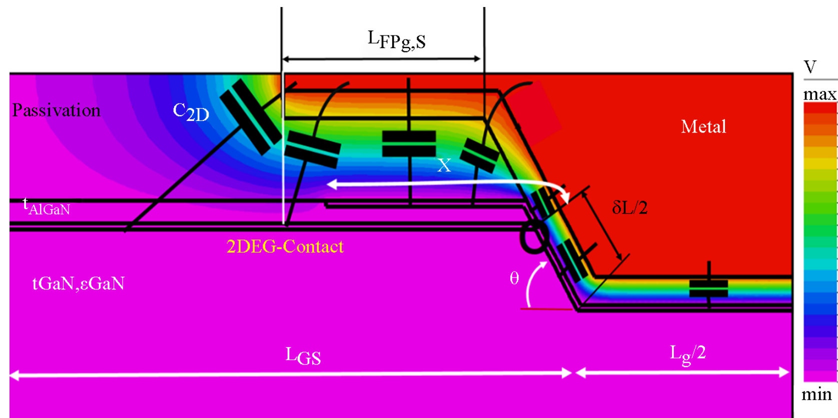

Figure 5. Potential map generated by simulation showing the parasitic coupling above the 2DEG region

We define the length *x* as the extension length of the second channel formed at the AlGaN/passivation interface from the AlGaN/Al_2O_3 interface. We can see its appearance in Figure 4b, but its extension may depend on many parameters (such as the gate field plate length, the bias and the polarization charge). Therefore, we will study the influence of this extension length x on parasitic coupling capacitances.

We also replaced the different semiconductor layers by dielectric layers having each time the same dielectric constant. The total capacitance was computed from Equation (1) where the total energy (Equation (2)) becomes $\varepsilon \cdot \varepsilon \Delta E^2/2$. Figure 5 shows the potential map and corresponding equivalent circuit of the coupling capacitance between metal and contact channel. Using different extension length x and $\delta L/2$ values, simulations allow us to estimate the parasitic coupling capacitance between the gate edge above the 2DEG and the access regions. In order to extract the parasitic capacitance from the simulation reported in Figure 5, we write:

$$C_{\text{Computed}}\left(\left(L_g+\delta L\right)/2, x, \theta, t_{\text{Pass}}, t_{\text{AlGaN}}\right)=C_{\text{ox}}\cdot\left(L_g+\delta L\right)/2+C_C\left(0, x, \theta, t_{\text{Pass}}, t_{\text{AlGaN}}\right) \tag{3}$$

where t_{Pass} and t_{AlGaN} are the thickness of passivation and AlGaN layers respectively. $C_{\text{ox}} \cdot (L_g + \delta \text{L})/2$ is the effective oxide capacitance (F/cm) in the active channel and $C_C(0, x, \theta, t_{\text{pass}}, t_{\text{AlGaN}})$ stands for all parasitic coupling capacitances. $\delta L/2$ is the gate side wall length, C_{ox} the oxide capacitance, θ the gate side wall angle and x the extension length of second channel.

Figure 6a shows the coupling capacitance $C_{\text{Computed}}(\delta L/2, x, \theta, t_{\text{pass}}, t_{\text{AlGaN}})$ at source side versus channel edge length $\delta L/2$ for various channel extension lengths x. The coupling capacitances depend linearly on $\delta L/2$ (Figure 6a) confirming the validity of Equation (3) definition. Therefore, $C_C(0, x, \theta, t_{\text{pass}}, t_{\text{AlGaN}})$ can be considered as a correct evaluation of coupling capacitance at source side. We must keep in mind that in the experimental measurements, the parasitic capacitance C_{Par} corresponds to parasitic coupling at both source and drain edges, which leads us to Equation (4).

$$C_{\text{Par}}(x) = 2 \cdot C_C\left(0, x, \theta, t_{\text{Pass}}, t_{\text{AlGaN}}\right) \tag{4}$$

Figure 6b shows the evolution of the different component of the parasitic coupling capacitance, $C_C(0, x, \theta, t_{\text{pass}}, t_{\text{AlGaN}})$ with the extension length x. C_C starts from 2.01×10^{-12} F/cm for $x = 0$ µm to 2.75×10^{-12} F/cm.

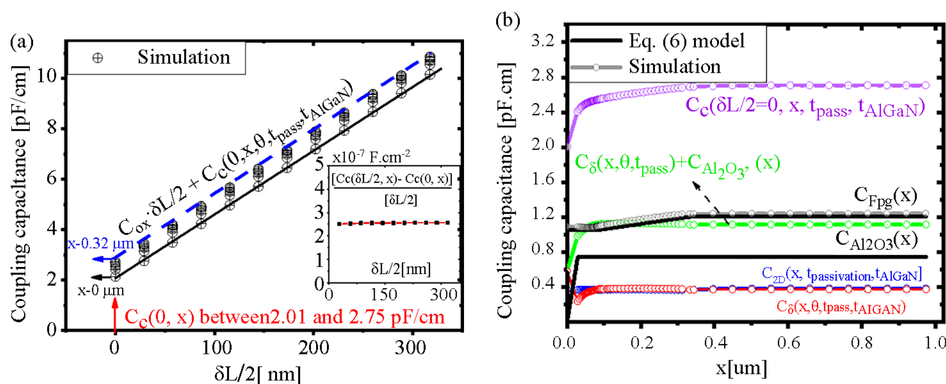

Figure 6. (a) Coupling capacitance versus $\delta L/2$ length and (b) parasitic coupling for $\delta L/2 = 0$ versus the length extension (x) of the second channel at the AlGaN/passivation interface

Figure 7 describes the simulated structure as well as the parameters we used for our model. We defined four successive extension regions of the parasitic channel, one at the AlGaN/Al_2O_3 and the others at the AlGaN/passivation interface. x_0, x_1, x_2 and x_3 are the respective contribution of the channel extension, $x = x_0 + x_1 + x_2 + x_3$ (x_2 is the coupling length under gate field plate and x_3 is the coupling length outside the gate field plate on the source or drain side). Depending on the extension of this parasitic channel, x can be equal to x_0, or $\frac{t_{\text{AlGaN}}}{\sin(\theta)}+x_1$, or $\frac{t_{\text{AlGaN}}}{\sin(\theta)}+\frac{t_{\text{Pass}}}{\tan(\theta)}+x_2$, or $\frac{t_{\text{AlGaN}}}{\sin(\theta)}+\frac{t_{\text{Pass}}}{\tan(\theta)}+L_{\text{FPg, s}}+x_3$. As

the methodology proposed here with Equations (1) and (2) calculates the coupling capacitance through the integral of all the local contributions (Equation (5)), it is possible to calculate the respective part of each region.

$$C_{\text{region}} = \frac{\left(\varepsilon \cdot \Delta E^2 + \Delta \rho \cdot \Delta V\right)}{\Delta V_g^2} \tag{5}$$

As a result, we propose in Equation (6) a simple model to estimate the parasitic coupling capacitance values $C_C(0, x, \theta, t_{\text{pass}}, t_{\text{AlGaN}})$.

$$\begin{aligned} C_C\left(0, x, \theta, t_{\text{Pass}}, t_{\text{AlGaN}}\right) &= C_{\text{FPg},1} \cdot \left(L_{\text{FPg,S}} - x_2\right) + C_{\text{FPg},2} \cdot x_2 + C_{\text{Al}_2\text{O}_3} \cdot x_0 \\ &+ C_{2\text{D}}\left(x_3, t_{\text{Pass}}, t_{\text{AlGaN}}\right) + C_\delta\left(x_0, x_1, \theta, t_{\text{Pass}}, t_{\text{AlGaN}}\right) \end{aligned} \tag{6}$$

where $C_{\text{FPg},1} \cdot \left(\left[\frac{1}{C_{\text{Al}_2\text{O}_3}} + \frac{1}{C_{\text{Pass}}} + \frac{1}{C_{\text{AlGaN}}}\right]^{-1}\right)$ and $C_{\text{FPg},2} \cdot \left(\left[\frac{1}{C_{\text{Al}_2\text{O}_3}} + \frac{1}{C_{\text{Pass}}}\right]^{-1}\right)$ are the coupling capacitances between gate field plate and electron channel at AlGaN/GaN or AlGaN/passivation interfaces, respectively. $C_{\text{Al}_2\text{O}_3}$ is the oxide capacitance (F/cm^2), C_{Pass} the passivation capacitance (F/cm^2) under the gate field plate and C_{AlGaN} the AlGaN layer capacitance. All of them follow $C = \varepsilon/t$ where ε and t are dielectric constant and thickness of each layer.

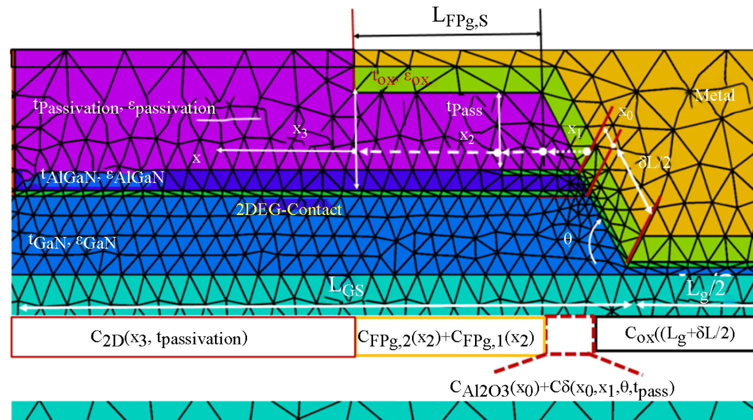

Figure 7. Structure used for the quasi-model used to evaluate parasitic coupling at source side ($L_{\text{FPg,S}}$ = 0.25 µm). θ is obtained from TEM-images (θ = 60° in our study)

In Equation (6), the first term $C_{\text{FPg},1} \cdot (L_{\text{FPg,S}} - x_2) + C_{\text{FPg},2} \cdot (x_2)$ is the coupling capacitance between the gate field plate and the electron channel, and it increases from 1.05 × 10^{-12} F/cm (if x = 0) to 1.2 × 10^{-12} F/cm for $x > \frac{t_{\text{AlGaN}}}{\sin(\theta)} + \frac{t_{\text{Pass}}}{\tan(\theta)} + L_{\text{FPg,S}}$. Depending on x_2, C_{FPg} accounts for 45% to 53% (x_2 = 0) of the total parasitic coupling. The second term $C_{\text{Al}_2\text{O}_3} \cdot x_0$ is the Al_2O_3 layer coupling between the gate edge and electron channel at AlGaN/Al_2O_3 interface, which increases from 0 to 7.42 × 10^{-13} F/cm when the whole parasitic channel is formed, accounting then for 27.5%. The third term $C_{2\text{D}}$ corresponds to the coupling between the gate field plate corner and access regions, it depends weakly on x_3, accounting for 14-15% of total parasitic capacitance. The last term $C_\delta(x_0, x_1, \theta, t_{\text{Pass}}, t_{\text{AlGaN}})$ is also a 2D coupling but this time in the proximity of the active channel, mainly in the extension regions corresponding to x_0 and x_1. It was obtained by subtracting all the previous contributions to the total coupling capacitance C_c (Figure 6b). C_δ accounts for 30% of the parasitic coupling in the case of no parasitic channel (x = 0) but decreases and saturates quickly to 14%, as the

parasitic channel increases. It should also be noted that, as the channel x_0 is formed along Al_2O_3 interface, the increase of $C_{Al_2O_3}$ from 0 to 27.5% is compensated by the decrease of C_δ, and the sum of them only varies from 30% to 41.5%. Thus, the variation of capacitances with x are moderate and the previous simulation (Figure 4b) has shown the formation of a parasitic channel in x_0 and x_1 regions.

After studying the total parasitic coupling capacitances $C_C(0, x, \theta, t_{Pass}, t_{AlGaN})$ by simulation or by the model of Equation (6), we can use the experimental capacitance measurements to estimate the difference ΔL_0(x) between the effective gate length L_{eff} and gate length L_g. We use the expression $L_{eff}(x) = C_{max}/W - C_{Par}(x)/C_{ox}$ (W in cm) [12], where C_{max} is the measured maximum capacitance and $C_{Par}(x)$ the simulated or modelled parasitic coupling capacitance Equation (4) for a 1 cm structure width.

Figure 8 shows different values of $\Delta L_0(x) = L_{eff}(x) - L_g$ versus gate length L_g for shallow and deep gate recess gates. The dashed lines in Figure 8 represent ΔL_0 measured by TEM, $\Delta L_{0,\,TEM} = L_{eff,\,TEM} - L_g$ (where $L_{eff,\,TEM} = L_{bottom} + 2(\delta L/2)$ obtained on MIS structures with 0.25 µm gate length for the deep gate recess wafer and a 0.5 µm gate length for the shallow gate recess wafer. We can see the good agreement between TEM physical extraction and simulation results, confirming the consistency of our study. Full device simulations (Figure 5) show the formation of a parasitic channel and the calculation of parasitic simulation $C_{Par}(x)$ agrees with the estimation of effective channel by TEM ($\Delta L_{0,\,TEM}$) measurement, especially when this parasitic channel is formed.

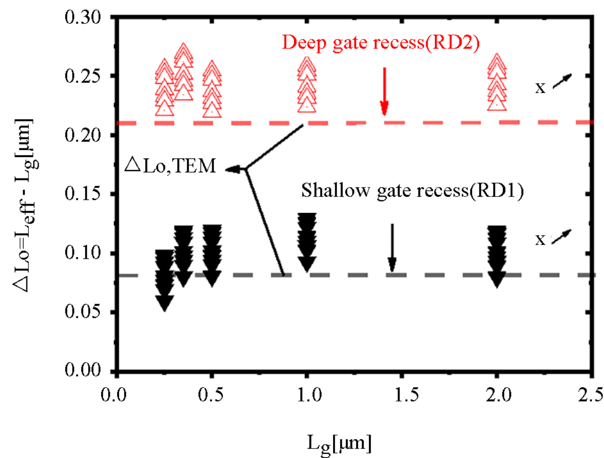

Figure 8. Difference $\Delta L_0 = L_{eff} - L_g$ versus L_g for shallow (RD1) and deep (RD2) gate recess of various parasitic coupling values corresponding to various x lengths

Figure 9 reports a CV measurement for a short channel GaN MIS-HEMT device with a deep gate recess (RD2), we can notice a double plateau behavior in the accumulation regime (note that this hump was also observed for RD1 device). This behavior is only visible on the shortest gate lengths for which it represents approximately 10% of the maximum capacitance. It could be due to the formation of the parasitic channel observed in simulation. The difference $\Delta C_{gc} = C_{gc}(V_g = 2V) - C_{gc}(V_g = 5\text{ V})/W$ is around 1.3 pF/cm (0.026 pF). This value is close to the parasitic coupling between gate and second channel, $C_{Al_2O_3}(x) + C_\delta(x, \theta, t_{Pass}, t_{AlGaN})$ obtained by simulation (1.2 pF/cm) confirming the hypothesis of such parasitic channel.

For a pragmatic use of this approach, capacitance measurements on a GaN MIS-HEMT device in accumulation can be employed to evaluate the effective channel length as long as the C_{Par} contribution to the effective channel capacitance is well understood and estimated. Two approaches are possible to estimate C_{Par}. It can be evaluated either by a full 2D semiconductor simulation (Figure 2) or using the analytical model proposed in Equation (6). We can also estimate C_{Par} on a specific structure using TEM analysis on a same MIS device for which capacitance measurement is also performed, based on maximum capacitance C_{max} in accumulation and $L_{eff,\,TEM}$. The parasitic capacitance is then obtained by $C_{Par} = C_{max} - C_{ox}{\cdot}W{\cdot}L_{eff,\,TEM}$. Figure 9a, b shows the corresponding equivalent circuit of the various capacitances discussed previously

in depletion and accumulation regimes. We indicated the location of gate-to-channel, gate-to-source and gate-to-drain capacitances, respectively C_{gc} (see Figure 9b), C_{gs} and C_{gd} (see Figure 9a).

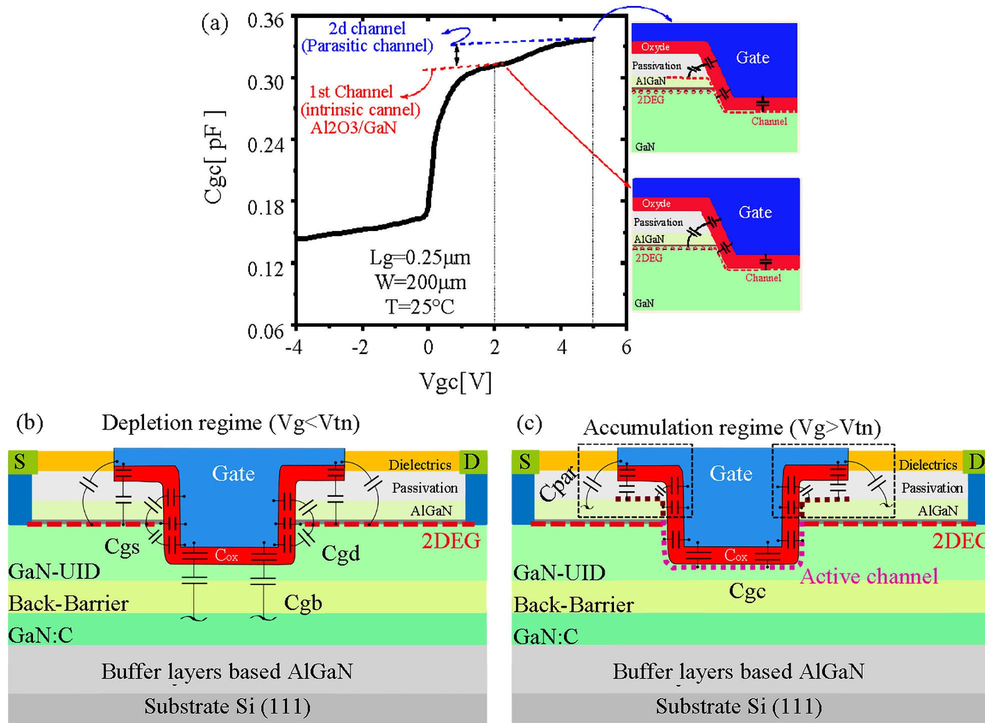

Figure 9. (a) Experimental gate-to-channel capacitance characteristics ($C_{gc} - V_g$) for deep gate recess device (RD2), showing the parasitic channel formation effect, (b, c) Corresponding physical equivalent circuit of the various capacitances respectively in depletion and accumulation regime

4. Conclusions

An in-depth analysis of parasitic coupling has been performed on GaN-HEMT devices with two different recess depths (RD1 and RD2) and various gate lengths. Extensive experimental capacitance analysis was completed and compared to 2D numerical simulations. A simple analytical model of the parasitic capacitances occurring at HEMT edges has been developed and validated with numerical simulations. The simulations also show the formation of parasitic channels at AlGaN/Al_2O_3 and AlGaN/Passivation interfaces. Moreover, the simulations clearly support the observation of different experimental parasitic capacitances observed both in depletion and in accumulation of electron channels. The proposed analytical model well predicts and explains the parasitic capacitance values and could be useful for reliable parameter extraction, device modeling and optimization. Finally, the results enable a reliable evaluation of the difference between the effective channel length (L_{eff}) and the gate length L_g, which is in very good agreement with physical lengths extracted from TEM images.

Acknowledgments

This work was partially supported by the French Public Authorities within the frame of the PSPC French national program “G-mobility”.

Data availability statement

The Figures data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of interest

The authors declare no conflict of interest.

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