



Article

More Than a Device: Function Implementation in a Multi-Gate Junctionless FET Structure

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Abstract: The miniaturization of the transistor sizes to keep up with Moore's Law in Integrated Circuits (ICs) is rapidly approaching the physical limits. To push the horizons of Moore's Law, among the various approaches available in the literature, single device-based computing shows promise by achieving more functionality in a smaller footprint. However, a single device-based computing approach either mainly embeds only the primitive logic hence inefficient in performance, or requires exotic devices like spin logic devices, and memristor which involve non-conventional costly manufacturing steps. Previously, we introduced the concept of embedding logic in a single device based on Crosstalk Computing, where deterministic signal interference between nano-metal lines is leveraged for logic computation. This paper elaborates upon the methodology of realizing complex Boolean functions through TCAD-based modeling and simulations, quantifying results, and compares against existing approaches. Core to our approach is a multi-gate Junctionless FET-based device, methodical placement of the independent gates, manipulation of device parameters, and dimension. This paper shows the implementation of various complex logic functions along with the primitive gates in the proposed device. Our benchmark results show 8x density benefits and 8x less power consumption on average than CMOS-based implementation. For the case of delay, elementary and complex logic devices show comparable characteristics with 14 nm PTM counterparts. Such realization of complex functions in a stand-alone device is compatible with the existing fabrication process.

Keywords: crosstalk computing, stand-alone device, independent gate, complex boolean function, multi-gate Junctionless FET

1. Introduction

The proliferation of Integrated Circuits (ICs) has played a vital role in global socioeconomic progress. With the slowdown of Moore's law [1–3], it is imperative to find solutions to continue this progress. Among various solutions available in the literature [4], embedding logic in a single device by manipulating device parameters provides one of the best possible alternative pathways [4–6]. Instead of having multiple devices for a Boolean logic unit, if a single device can exhibit the Boolean function itself, the ensemble will collapse down to the footprint of a single device. However, such approaches are mostly confined to embedding only primitive cells like NAND/NOR in a single device and show a small number of density benefits [7,8] or include exotic devices like Complimentary Resistive Switch [4] and Bipolar Memristors [5]. Hence, require costly non-conventional manufacturing processes [6].

We propose implementing Boolean complex logic in a stand-alone device similar to multi-gate Junctionless FET by utilizing a novel computing technique called Crosstalk Computing [8]. In Crosstalk Computing, metallic

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nano-lines acting as aggressors are organized in a compact manner such that whenever signal transitions take place in these lines, the sum of their crosstalk interference gets induced through virtual coupling capacitance in another metal nano-line called victim; the transitioning signals are inputs, and the net induced charge is the output. The coupling strength between the input and output metal lines and the net charge induced determines what logic is computed. We resemble this aggressor-victim scenario in our proposed multi-gate Junctionless device where independent gates act as aggressors and the silicon fin of the device act as a victim. By placing the independent gates within the device astutely, we can control the formation of accumulation or inversion in the device fin to get the saturation current at the output. Device geometry, placement of gates, and manipulation of the device parameters are the keys to achieve the desired logic function.

Previously, we introduced the concept of implementing logic functions in a single device by exploring Crosstalk Computing technology but was only limited to primitive gates [8]. This paper has detailed the methodology of implementing complex Boolean functions in a single device. We have implemented the device using Technology Computer-Aided Design (TCAD) SProcess [9]. For the characterization of the device and verification of the Boolean functionality, we have used TCAD SDevice [10]. Extending our previous work, the key contributions of this paper are as follows:

- Details of fabric construct include material aspects, geometric parameter variation, dimension, usage, and overall integration of Boolean functions.
- Discussion of fabric-specific Boolean function mapping scheme with examples like basic and complex logic.
- Details of device characteristics and analysis of I_{ON} and I_{OFF} current for identifying a logic state of a Boolean function.
- Evaluation of density, power, and delay performance concerning existing work available in the literature and existing 14 nm CMOS technology.

We have implemented two primitive gates (AND, OR) and two complex Boolean functions ($AB+BC+CA$ and $B+AC$). Our results show and verify the functionality of logic gates. Our comparison results also show that for the primitive gates, there is 6x density gain and, on average, 8x average power reduction. For complex functions, the average density benefit is 13x, the average power reduction is 10x, and the delay is also in good agreement concerning CMOS counterparts.

The rest of the paper is organized as follows: Section 2 discusses the approach for embedding the device's functionality. Section 3 illustrates the methodology evaluation; Sections 4 and 5 discuss the detailed result of implemented complex logic and compares results. Finally, Section 6 concludes the paper.

2. Approach for Embedding Functionality of the Device

We have followed a bottom-up modeling approach where a multi-gate Junctionless FET is used as the core functional unit. Control of independent gates, utilization of inversion/depletion mode, and customization of the device parameters are the keys to performing the logic operation in the single proposed device. The device is first implemented in the Sentaurus TCAD process and then characterized using the TCAD device simulation in our bottom-up modeling approach. From device simulation, ON current is achieved through the I-V characteristics of the device for identifying the logic state. For implementing Boolean functionality in the device, the Crosstalk Computing concept is considered for its high-density benefit [8]. To reassemble the Crosstalk Computing, independent gates of the device will act as aggressors, and the fin will act as a virtual victim. Like the interference-based aggressor-victim scenario, when voltage is applied at the gate, based on the voltage level, the device will either work in the inversion or depletion region. For the voltage below the threshold voltage, the device will remain in the depletion region and be in a partial ON state and produce logic 0 as output. For the voltage above the threshold limit, the device will be in the inversion region and be in an entirely ON state and produce logic 1 as output. Following this principle, elementary and complex logic are implemented in the device. In this paper, inputs A, B, and C are mapped to gate-1, gate-2, and gate-3, respectively. The selection of gate material and the gate dielectric is considered by reviewing numerous references [11–24]. TiN is considered as gate material for its specific work function of 4.4 eV. As mid-bandgap metal TiN, its work function is varied from 4.4 to 4.6 eV because of granularity. Tuning the work function, and proper potential barriers can be implemented for gate control. HfO_2 is selected as the gate dielectric for its high dielectric constant which is essential for tuning the gate potential as well as gate control. Considering these issues, the device is implemented in SProcess and SDevice.

2.1 Elementary Logic

Two independent gates based on Junctionless FET implement the elementary logic gates (OR & AND). Input voltage is applied at the independent gates by voltage sweeping; in this case, Gate-1 (Input A) and Gate-2 (Input B) (Figures 1(i & ii)). When the voltage is applied in the subthreshold, charge is depleted in the silicon fin. When some part of the Silicon fin (Figure 1(i(a))) becomes neutral (i.e, no more depletion), then the threshold voltage is reached, and bulk current starts to flow in neutral silicon [6]. As the depletion decreases with the gate voltage increase, the diameter of the neutral channel also increases. At this moment, the device is in inversion (Figures 1(i(b-d))). When the device reaches flat band voltage, the entire channel region becomes neutral (Figure 1(i(d))). Further increment of voltage will lead to full inversion. Here two gates act as aggressors, and the silicon fin acts like a victim, which resembles a Crosstalk setup.

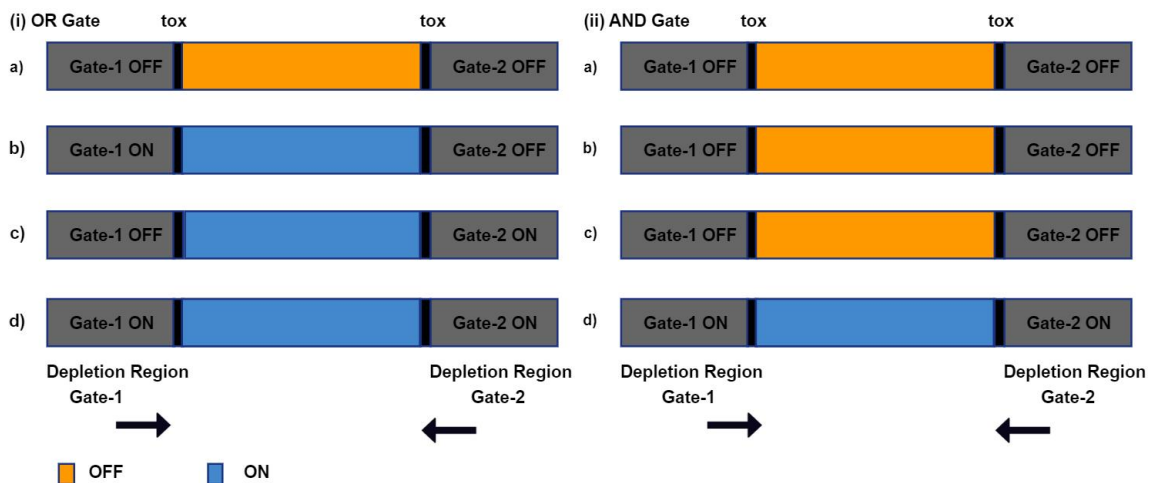


Figure 1. Switching Mechanism of elementary gates for several switching conditions i) OR gate ii) AND gate. In both cases, depletion, partial inversion, and inversion occur for switching conditions.

For example, in two input OR logic, when both the gates are ‘OFF,’ the depletion region beneath these two gates will overlap with each other. Hence, no current will flow, and the output will be logic 0, depicted in Figure 1(i(a)). However, when one of the gates is ‘ON’ and the other is ‘OFF,’ the depletion region will be removed, and partial inversion will occur, resulting in a conduction path (channel) between the source and drain (Figures 1(i(b-c))). The device will then be in the ‘ON’ state, and the output will be logic 1. When both the gates are ‘ON,’ and the drain voltage is constant, the depletion region completely disappears, and full inversion will take place, widening the channel path to get a fully ON state and producing logic 1 output (Figure 1(i(d))).

Similarly, for AND operation, when both gates are in an ‘OFF’ state, depletion regions will overlap, as shown in Figure 1(ii(a)). For one of the gates is ‘ON,’ the depletion region will wither away from the respected ‘ON’ gate area because of voltage increments and proceed to the inversion. However, the depletion region will remain at the ‘OFF’ state. As a result, the transistor will remain in the ‘OFF’ state (Figures 1(ii(b-c))). Only the specific voltage above the threshold voltage at both gates will remove all depletion regions, and the transistor will be in the ‘ON’ state (Figure 1(ii(d))).

We proposed a double gate Junctionless device based on the above principle as shown in Figure 2 with 2 input AND, OR gates Figures 2(a & b) illustrate OR device and log plot of I-V characteristics, respectively. From Table 1, the device has a gate length of 14 nm, the gate material is TiN, a silicon fin width of 20 nm, and 20 nm in height. The device has an ON current of 10 μ A and an OFF current of 0.32 pA with a threshold voltage of 0.3 V (Figure 2b). As can be seen from Figures 2(a & c), the main differences between AND, OR devices are the orientation of the two independent gates. For OR logic implementation, the gate lengths are placed across each other to have equal control of the channel. Due to such arrangements, any individual gate or both gates together can create a partial inversion region within the channel (logic 1 at the output) whenever an input voltage is applied to the gates. In contrast, AND device gates’ location is diagonal to each, which ensures the AND operation.

Table 1. Device dimensions for implementing the different logic function

Proposed Device	Fin Width (nm)	Fin Height (nm)	Gate-1,3 Oxide Thickness (nm)	Gate-2 Oxide Thickness (nm)	Gate Length (nm)
AND	20	20	2 (Gate-1)	2 (Gate-2)	14
OR	20	20	2 (Gate-1)	2 (Gate-2)	14
AB+BC+CA	22	20	9	3	14
B+AC	42	20	9	3	14

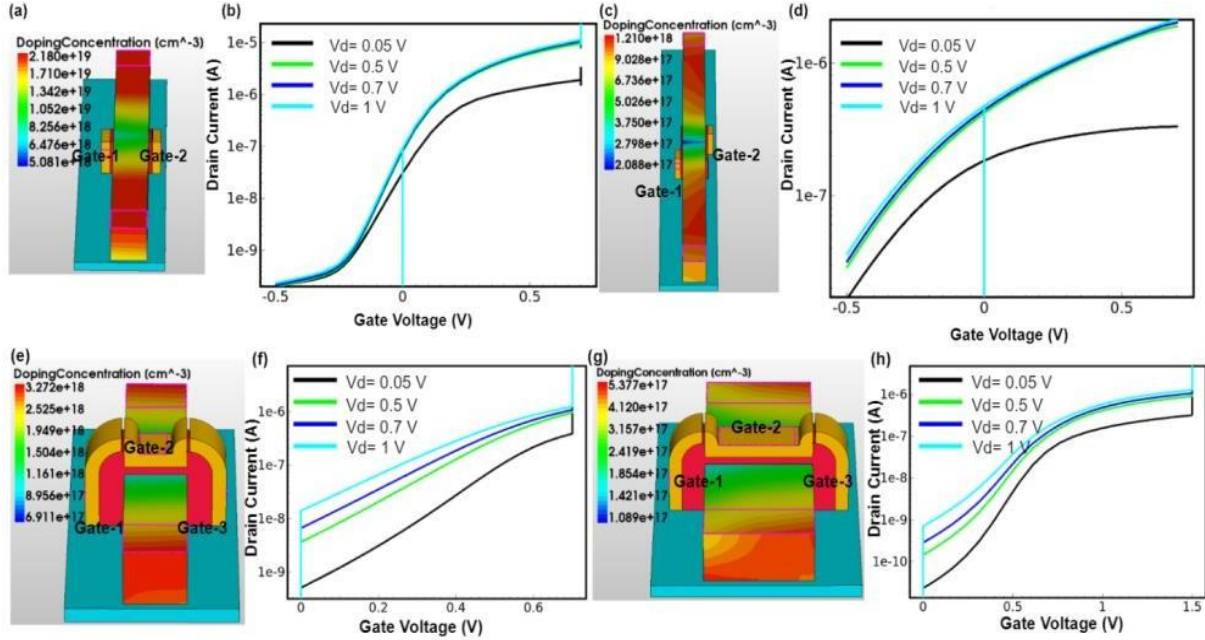


Fig 2. The device structure of proposed Junctionless FET where elementary logic and complex logic are implemented a) OR logic device structure; b) Log plot of I-V characteristics of OR logic gate; c) Device structure of Junctionless FET where AND logic is implemented; d) Log plot of I-V characteristics of AND logic device; e) Device structure of AB+BC+CA logic implemented device; f) Log plot of I-V characteristics of AB+BC+CA; g) Device structure of B+AC implemented device; h) Log plot of I-V characteristics of B+AC device.

Figure 2c shows AND gate where the device has a gate length of 14 nm, silicon fin height of 20 nm, and 20 nm silicon width. I-V characteristic of the device in which AND gate is implemented is given in Figure 2d. From the log plot of I-V characteristics of AND device (Figure 2d), it can be found that the ON current of the device is 1 μA and OFF current is 1 pA with a threshold voltage of 0.25 V. Detail dimension of the device is provided in Table 1. For AND logic implementation, gates are placed on the opposite side, far away from each other. As a result, if any single gate has logic 1 input, it will not have enough control over the fin to create partial inversion and, therefore, will generate logic 0 at the output. However, when both gates have logic 1 input, the device will move from the depletion region to the partial inversion region and produce logic 1 output.

Implementing geometric parameters from Table 1, AND, OR device is modeled. Table 2 lists the total current for all input combinations for both 2 input AND, OR logic. For the 00-input combination, AND produces 1 pA, and OR is producing 20 pA and stay in OFF state. For 01 and 10 input combinations, AND device has a total current of 25 nA, which is less than the ON current obtained from the device I-V characteristic because of gate orientation. However, for the OR device, the total current is 10 μA which is greater than the AND device's ON current and creates ON state (logic 1) at the output. For logic 1 input in both gates, the AND device has a total current of 1 μA and reaches the ON state. OR is drawing 20 μA and stays in ON state.

Table 2. Elementary Logic Total Output Current

Gate-1 Logic Input	Gate-2 Logic Input	OR Gate Total Current (A)	AND Gate Total Current (A)
0	0	2e-11	1e-12
0	1	1e-5	2.5e-8
1	0	1e-5	2.5e-8
1	1	2e-5	1e-6

2.2 Complex Logic

Figures 2(e & g) show the implementation of two different complex Boolean functions, $AB+BC+CA$ and $B+AC$, respectively. Both devices have three independent gates based on the number of inputs of the logic functions. Using Crosstalk Computing technology, three independent gate-based Junctionless devices can efficiently implement different complex multi-level logic functions. $AB+BC+CA$ and $B+AC$ are such complex multi-level logic functions. The logic function $AB+BC+CA$ is the expression for a full adder carry function. Hence, a full adder can be produced using this device. The device can be customized based on the input configuration of the logic function. The customization includes varying the gate location and gate oxide thickness [8].

Implementation of Boolean Function $AB+BC+CA$ is shown in Figures 2(e & g). Device dimensions are given in Table 1. For this function, the output will be logic 1 when at least two inputs transition from low to high. We customized the device with three equal independent gates to achieve this functionality. All the gates are of equal length and contribute to the fin of attaining partial inversion. However, the oxide thickness for the gates is chosen to be different to limit the excess current flow during switching activities. Our previous work [8] shows that by keeping all other parameters the same, current flow can be limited by increasing doping concentration and gate oxide thickness. Oxide thickness for Gate-1 (Input A) and Gate-3 (Input C) is kept at 9 nm to limit excess current generation, and for Gate-2 (Input B), gate oxide thickness is 2 nm. HfO₂ has been used as a gate oxide. This Junctionless FET has a gate length of 14 nm and a fin width of 22 nm with a height of 20 nm Figure 2f is the log plot of the I-V characteristic of the device. The device has an I_{ON} of 2.2 μ A and I_{OFF} of 1e-10 A/ μ m with a threshold voltage of 0.53 V.

Figure 2g depicts the device structure to realize the $B+AC$ logic function. This device has a fin width of 42 nm, a fin height of 20 nm, and a gate length of 14 nm made of TiN. HfO₂ is used as a gate oxide for this device as well. Gate-1 (Input A) and Gate-3 (Input C) have a gate oxide thickness of 9 nm, and Gate-2 has 2 nm. Figure 2g exhibits the log plot of the I-V characteristics of the device. The device has an ON current of 1.2 μ A and an OFF current of 6.5e-10 A with a threshold voltage of 0.53 V. To comply with the $B+AC$ logic condition, we increase the width of the fin. As a result, Gate-2 (Input B) will have a wider area to control inversion/partial depletion [10]. The other two gates will equally contribute to producing current. In this device, Gate-2 (Input B) should produce more current than Gate-1 (Input A) and Gate-3 (Input C). To present Gate-2 (Input B) is made intentionally wider with 2 nm oxide thickness so that it will work as a dominant gate/input to produce more current, and Gate-2 will achieve inversion faster than the other two gates and fulfill the logic. Gate-1 and Gate-3 have shorter gate areas than Gate-2, and current is also limited with 9 nm oxide thickness. Such gate arrangement is made to fulfill the logic of $B+AC$. The same Crosstalk setup is also applied here. Here, three gates act as aggressors, and the silicon fin acts like a victim.

3. Methodology

To achieve a functioning device, it is essential to examine the electrical characteristics. The device is designed with Sentaurus Process, which imitates the physical process steps. Obtaining the device by Synopsys Sentaurus Process [9], characteristic analysis is done with the Sentaurus Device [10]. The Sdevice model solves Poisson and carrier continuity equation to determine current behavior characterization. The silicon band structure and the effect of bandgap narrowing are calculated by the Oldslotboom method. From I-V characteristics, ON current, and OFF current is extracted and by examining the value of ON current, logic 0 and logic 1 are determined. the AC and DC behavior of a device cumulate the overall performance of a device (Table 3). For examining DC and AC characteristics of a device, average power, leakage power, and delay are crucial parameters. Average power and leakage power were extracted from the I-V characteristics using the basic formula for power. Propagation delay is calculated using the equation given in [13]:

$$\text{Delay, } \tau = C_g * V_{dd} / I_{on} \quad (1)$$

C_g is gate capacitance, V_{dd} is drain voltage, and I_{on} is ON current. Considering the condition of ON, the current of 1 μ A is regarded as logic 1. CMOS counterpart 14nm PTM I_{ON} and I_{OFF} are extracted from HSPICE simulations. Average power and leakage power are also extracted from the HSPICE simulation. To get the proper propagation delay of the PTM devices, the critical path of the circuit is considered and calculated from HSPICE. The Proposed devices and 14 nm PTM CMOS counterpart power and delay are summarized in Tables 4 and 5.

4. Results and Discussion

The present study confirms the findings of functional implementation in a standalone device (Figures 2(a & c), Figures 2(e & g)) and shows the devices' efficiency in multi-gate functionality. Together, the present findings ensured the validity of our proposed devices AB+BC+CA and B+AC as complex logic.

Figure 3i depicts some selected cases of input combination (000, 010, 100, 101, 110, and 111) for the AB+BC+CA logic, and Table 3 lists all the possible input combinations, the current of corresponding gates, and total current. For the logic 1 output, we considered $1e-7$ A as the threshold current and acquired AB+BC+CA logic. For logic 0 input in all gates, inversion regions overlap with each other, and as a result, the device will be in weak inversion, producing $1e-10$ A at the output; hence, the device is in the 'OFF' state. For logic 1 input in only one gate, the same incidents happen; the device produces a $5.2e-8$ A output current and remains in the 'OFF' state. For logic 1 input in two gates of 011, 110 and 101 switching conditions, the inversion regions withered away, and conducting channel established between the source and drain produced an output current of $8.5e-7$ A. As a result, the device shifted to the 'ON' state. The same phenomena occurred for the logic 1 input in all three gates. The device produces an output current of $2 \mu\text{A}$ and produced a logic 1 output.

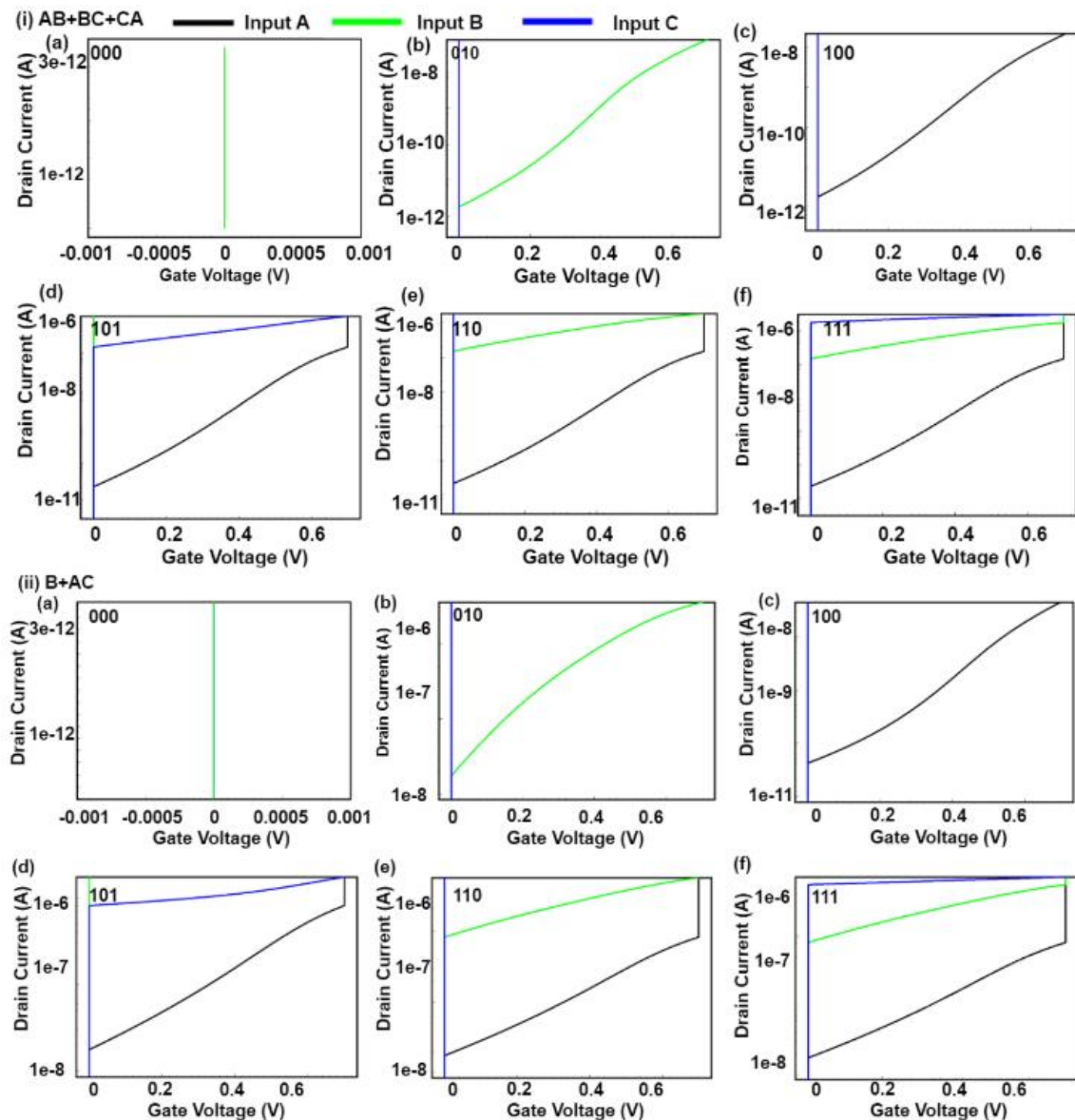


Figure 3. Log plot of I-V characteristics of several switching cases of complex logics (i) AB+BC+CA logic Here I-V plot corresponding to a) 000 input; b) 010 input; c) 011 input; d) 101 input; e) 110 input; and f) 111 input; (ii) Log plot of I-V characteristics of B+AC logic Here I-V plot corresponding to a) 000 input; b) 010 input; c) 011 input; d) 101 input; e) 110 input; f) 111 input. Here gate-1, 2, and 3 correspond to Input A, B, and C respectively.

Figure 3ii depicts some selected input cases for B+AC logic, and Table 3 enlists all the current outputs corresponding to gates and total current. From Table 3, it can be seen that for the logic 0 input in three gates, the gate could not get enough control to achieve inversion, and subsequently, the device remains in the depletion region and draw a current of $1e-10$ A; hence, logic 0. The same scenario happened for logic 1, for input combinations 001 and 100. For each case, the device remains in the depletion region and produces a $5.7e-8$ A output current; hence, OFF state. In the case of the 010 input, the device has a $5.5e-7$ A output current and produces a logic 1 output. In this device, gate 2 is the dominant gate. During the high transition of the input signal, the device goes in the partial inversion region; hence ON state (i.e. logic 1 output). For 011, 101, and 110 input combinations, since multiple inputs are high, the device goes to the partial inversion region and produces a logic 1 at the output. For all 011 and 101 input cases, the device has a $1.6 \mu\text{A}$ output current. The same scenario can be seen for the 111 input; the device gets a logic 1 output due to partial inversion and produces $2.5 \mu\text{A}$ total output current from three gates.

From Table 3, it is observed that all the switching cases are the same except the 010 input, where we are getting a logic 1 output. For the second device, the wider Gate-2 acts as the dominant gate and controls the channel, guiding it towards the partial inversion state. Both figures show that with multiple high inputs like 011, 101, 110, and 111, one gate acts as a dominant gate, aggregates all the currents from the other gates, and produces the total current.

Table 3. Elementary Logic Total Output Current

Device	Gate-1 Logic Input (A)	Gate-2 Logic Input (B)	Gate-3 Logic Input (C)	Current (G-1)	Current (G-2)	Current (G-3)	Total Current
AB+BC+CA	0	0	0	$1e-10$	$1e-10$	$1e-10$	$1e-10$
	0	0	1	$1e-10$	$1e-10$	$5.2e-8$	$5.2e-8$
	0	1	0	$1e-10$	$6.3e-8$	$1e-10$	$6.3e-8$
	0	1	1	$1e-10$	$7e-8$	$8.5e-7$	$8.5e-7$
	1	0	0	$5.2e-8$	$1e-10$	$1e-10$	$5.2e-8$
	1	0	1	$5.2e-8$	$1e-10$	$4e-7$	$4e-7$
	1	1	0	$5.2e-8$	$8.5e-7$	$1e-10$	$8.5e-7$
B+AC	1	1	1	$5.2e-8$	$8.4e-7$	$2e-6$	$2e-6$
	0	0	0	$1e-10$	$1e-10$	$1e-10$	$1e-10$
	0	0	1	$1e-10$	$1e-10$	$5.7e-8$	$5.7e-8$
	0	1	0	$1e-10$	$5.5e-7$	$1e-10$	$5.5e-7$
	0	1	1	$1e-10$	$5.2e-7$	$1.2e-6$	$1.2e-6$
	1	0	0	$2.5e-8$	$1e-10$	$1e-10$	$2.5e-8$
	1	0	1	$2.5e-8$	$1e-10$	$1.5e-7$	$1.5e-7$
1	1	0	$2.3e-8$	$1.4e-6$	$1e-10$	$1.4e-6$	
1	1	1	$2.3e-8$	$1.4e-6$	$2.5e-6$	$2.5e-6$	

Average power, leakage power, delay, and Power Delay Product (PDP) are also calculated for the proposed devices of AND, OR, AB+BC+CA, and B+AC and compared with CMOS 14 nm devices and presented in Tables 4 and 5. Considering average power, the AND logic circuit and the OR device consume $0.3 \mu\text{W}$ and $0.115 \mu\text{W}$ where 14 nm PTM AND, OR consume $3.74 \mu\text{W}$ and $6.19 \mu\text{W}$, respectively. The difference is mainly because of the transistor count reduction in the proposed device. The proposed device is a single device with functionality whereas the CMOS counterpart consists of several transistors with more resistive paths. As a result, the CMOS counterpart will consume much more power during multiple switching events than the proposed device. Leakage power for the AND device and the OR device is 0.064 nW and 0.016 nW , respectively. Both the devices have very small OFF currents 0.92 nA and 0.023 nA , respectively, resulting in this minimal leakage power. For the case of 15 nm Junctionless Single Gate Tunneling FET (JLSGTFET), ON current is $9.91e-4 \text{ A}$ and OFF current is $2.8e-13 \text{ A}$ [25].

The reason for minimal leakage power is also transistor count. For the 14 nm PTM counterpart, the transistor count is greater than the proposed device. Transistors count along with the resistive path, increasing leakage power. Our proposed AB+BC+CA device and the B+AC device have a leakage power of 0.098 nW and 0.412 nW , respectively, where 14nm PTM counterparts have 0.574 nW and 0.373 nW . The reason for this small leakage power is the tiny OFF current of our proposed device. The AB+BC+CA and B+AC device has a delay of 11.84 ps and 25.51 ps , respectively. The larger width of the B+AC device causes this longer delay than the AB+BC+CA device. 14 nm PTM counterpart has a 59.48 ps and 61.1 ps delay for AB+BC+CA and B+AC, respectively. This time delay is calculated considering the critical path netlist. The proposed research AND, OR devices delay 4.45 ps and 3.93 ps , respectively. As the proposed AND device has a small gate length, it will take a longer time to achieve partial depletion. So, the proposed AND device has a longer delay than the proposed OR device. The 14nm PTM AND, OR delay 37.19 ps and 29.49 ps , respectively. While considering power, it is

recorded that our proposed devices consume less power than the 14nm PTM AND, OR devices. Our proposed device delay is in good agreement with the CMOS counterpart.

Table 4. Power, Delay, and Density Comparison of Elementary Logics

	AND (14nm PTM)	AND (Proposed Device)	OR (14nm PTM)	OR (Proposed Device)
Average Power (μ W)	3.74	0.3	6.19	0.115
Leakage Power (nW)	0.346	0.064	0.2	0.016
Delay (ps)	37.194	4.45	29.49	3.93
Transistor Count	6	1	6	1
Area (μ m ²)	0.047	0.037	0.047	0.037
PDP (J)	1.39e-4	1.34e-6	4.52e-7	1.83e-4

Table 5. Power, Delay, and Density Comparison of Complex Logics

	AB+BC+CA (14nm PTM)	AB+BC+CA (Proposed Device)	B+AC (14nm PTM)	B+AC (Proposed Device)
Average Power (μ W)	9.1	0.6	6.8	1.45
Leakage Power (nW)	0.574	0.098	0.373	0.412
Delay (ps)	59.48	11.84	61.109	25.51
Transistor Count	20	1	8	1
Area (μ m ²)	0.13	0.062	0.062	0.062
PDP (J)	5.41e-4	7.1e-6	4.16e-6	3.7e-5

Power Delay Product (PDP) indicates the average energy consumed per switching. Regarding our proposed device, AND, OR devices have PDP of 1.34e-6 J and 1.83e-6 J, and CMOS counterparts have much higher PDP because of transistor number. The same case goes for complex logic. Our proposed devices have less PDP than CMOS devices.

Achieving such Crosstalk logic behaviours in a single device indicates a denser circuit design. From the proposed methodology, it is evident that the device consists of lesser transistors with significant benefits. The AB+BC+CA logic circuit will require only one transistor, whereas CMOS technology will involve twenty transistors in the proposed device. For the case of B+AC Logic, the proposed research requires one transistor, where CMOS technology involves eight transistors. In the proposed research, the AB+BC+CA logic circuit space occupation is 10 times smaller compared to the CMOS counterpart regardless of the technology node. For B+AC logic, it is 3 times smaller than the CMOS counterpart. Regarding power, it consumes 8x times less average power than existing CMOS architecture, and the time delay is in picoseconds for both of our proposed devices which can be considered high-speed devices.

5. Random Dopant Fluctuation Analysis

Random dopant fluctuation (RDF) is analyzed for junctionless devices with TCAD [14]. RDF is a kind of process variation that occurs from implanted impurity concentration. RDF causes threshold voltage fluctuation, degradation of ON current, and increment of OFF current. RDF effect is simulated on elementary logic devices and complex logic devices.

Considering elementary logic, AND device is selected. Regular AND devices with RDF are compared with On current and Off current. The discrete random dopants are varied from 100 to 500, and performances are compared in Table 6. From this table, the regular AND device and RDF devices have the same current range with fluctuation. For 00 switching conditions, the device with 400 discrete particles has the highest current but is acceptable. For 01 switching condition, the device with 200 discrete dopants has the highest current limit.

In every case, some devices get a little bit extra current. The reason is that all the devices with RDF and the regular devices have the same doping concentration. For threshold voltage, the same reason is applicable.

AB+BC+CA device is analyzed with RDF as a complex logic device in Table 7. The device was analyzed with varying discrete dopants from 100 to 500 particles. Compared with the regular device, the devices with RDF are working in the proper current range with a slight fluctuation. The threshold voltage remains the same for the regular device and all cases of RDF. Both ON current and OFF current are in the proper range. For the 011 switching case, the device with 100 discrete particles has the maximum current in the acceptable range. For the 111 switching case, the device with 200 discrete dopants has the highest current in the range. As all the devices are junctionless devices with the same doping concentration all over, that plays a significant role in

retaining an acceptable range of current, and very small scale of current fluctuations occur for random dopant effect.

Table 6. Comparison of regular AND device and RDF-affected device

Switching Case	Regular	100 Particles	200 Particles	300 Particles	400 Particles	500 Particles
00	1e-12	1e-12	1e-12	1.5e-12	4e-12	1e-12
01	1.4e-8	7.2e-8	8e-8	2.4e-8	6.8e-8	1e-8
10	7.7e-8	6.4e-8	7.5e-8	7.7e-8	8e-8	9.3e-8
11	1.5e-6	1.3e-6	1.3e-6	1.2e-6	1.2e-6	1.2e-6
On Current (A)	1.5e-6	1.3e-6	1.3e-6	1.1e-6	1.1e-6	1.2e-6
Off Current (A)	7e-15	7.7e-15	6e-15	2e-15	2e-14	2e-15
V _i (V)	0.45	0.45	0.45	0.45	0.45	0.45

Table 7. Comparison of regular AB+BC+CA device and RDF-affected device

Switching Case	Regular	100 Particles	200 Particles	300 Particles	400 Particles	500 Particles
000	1e-12	6e-12	2e-12	1e-12	1e-12	6e-12
001	8e-8	8.8e-8	9e-8	9e-8	7e-8	8e-8
010	8e-8	8e-8	6e-8	8e-8	9e-8	9e-8
011	1.5e-6	3.3e-6	1.8e-6	1.2e-6	1.5e-6	1.5e-6
100	7e-8	4.7e-8	3e-8	4e-8	7e-8	4e-8
101	1e-6	1.2e-6	1e-6	1e-6	1e-6	1.3e-6
110	1.5e-6	1.5e-6	1.5e-6	1.5e-6	1.3e-6	1e-6
111	2e-6	1.5e-6	3e-6	1.8e-6	2.5e-6	2.6e-6
On Current (A)	2.8e-6	2.5e-6	3.4e-6	1.6e-6	2.8e-6	2.2e-6
Off Current (A)	1.8e-11	1.1e-11	2.7e-11	4e-12	1.8e-11	6e-12
V _i (V)	0.69	0.69	0.69	0.69	0.69	0.69

Although the RDF problem can be solved, there will be some difficulties with our proposed device. The devices will be hard to fabricate as their gate length is minimal, and the gate location must be precise to get logic output. Hence, there is some fabrication complexity with these proposed devices. Adjacent devices will affect the performance of each other if they are located too close. As a result, a particular distance between devices should be maintained to get noise-free output. Scaling down of devices may affect the noise margin of the devices. These complexities remain in our proposed devices.

6. Conclusion

Embedding functionality in a single device is a novel way of performing logic computations. In this paper, we proposed a new scheme for implementing the device as a functional component. The paper presents a detailed framework for the device structure necessary to achieve different logic functionality in a standalone device. Previously, we implemented a primitive gate in a single device. We implemented complex logic, AB+BC+CA, and B+CA in single devices and demonstrated their functionality in this work. The devices are also examined in random dopant fluctuation, and the devices are performing well in the RDF condition. This standalone device approach can yield a higher density of benefits of 8x compared to the conventional CMOS technology, and power consumption is 8x lesser than the CMOS counterpart. The device delay of the elementary and complex logic devices is comparable with 14nm PTM counterparts and exhibits better performance and promises better performance in all issues.

Conflict of interest

There is no conflict of interest for this study.

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