Journal of Electronics and Electrical Engineering
https://ojs.wiserpub.com/index.php/JEEE/

UNIVERSAL WISER PUBLISHER

Article

Performance Optimization of Carbon Nano-Tube Field Effect Transistors by Tuning Parameters

Kriti Rai Saini, Shailesh Rajput*, Yoonsuk Choi

Department of Electrical and Computer Engineering, California State University, Fullerton, CA, USA
E-mail: shaileshrajput@csu.fullerton.edu

Received: 12 September 2022; **Revised:** 20 October 2022; **Accepted:** 20 October2022

Abstract: As transistors are scaled down to keep up with Moore's law, the semiconductor industry is facing several challenges due to the limitation of traditional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology. To overcome this issue of scalability, various other technologies are being researched. Among them are Carbon Nano-Tube Field Effect Transistors (CNTFET), Ribbon Field Effect Transistors (RibbonFET), Graphene Nanoribbon Field Effect Transistor (GNRFET), and Fin shaped Field Effect Transistor (FinFET), which can substitute MOSFETs. Due to carbon nanotubes' excellent conductivity supremacy, CNTFETs are a promising new solution. However, implementing a CNTFET and making circuits from it is still challenging as CNTFETs can exhibit properties of both semiconductor and metal depending on various parameters. This paper will illustrate the characteristics of the CNTFET, compare the power consumption and propagation delay of basic logic gates made using the CNTFET and MOSFET technology. The parameter tuning is done by measuring the power and delay for all parameter values. The Simulation of CNTFET is done on the Stanford CNTFET model using H-Spice.

Keywords: CNTFET, PDP, physical parameter tuning

1. Introduction

A Carbon Nanotube (CNT) is a cylindrical rolled structure of a graphene sheet, an allotrope of carbon. Transistors made using CNT as the channel between source and drain, are known as CNTFET. The CNT is divided into two types, namely the Single-Walled CNT (comprising of one CNT between the source and the drain), and Multi-walled CNT (coaxial set of multiple hollow CNTs between the source and the drain). CNTFET has the physical channel, unlike the conventional MOSFET, where the channel is induced between the source and the drain due to the applied gate voltage [1].

With respect to the structural arrangement, the carbon nanotube is further classified as i) Armchair, ii) Zigzag, and iii) Chiral. The semiconducting or metallic properties of CNTs are determined by the structural arrangement of the CNT atom and chirality, i.e., a combination of chiral vector and chiral angle. The CNTs are metallic if the chiral index, follows the condition m = n or m−n = 3i, where i is an integer, while for other values of m and n vector, CNTs are semiconductors. The conductivity of CNTs is around 80 times higher than that of copper, and the electron and hole mobility is better than silicon, resulting in quasi-ballistic charge carrier transport in a carbon nanotube. With all the promising features of CNTFETs, this device seems advantageous over traditional MOSFET devices in terms of propagation delay and Power Delay Product (PDP).

DOI: https://doi.org/10.37256/jeee.1120221926

2. Literature Review

As we continue scaling down MOSFETs, various undesirable effects, like source to drain tunneling and short-channel effects (SCE) due to decrease in gate length and lack of control over leakage current, are introduced. The mobility of electrons is also impacted when the channel length is decreased in MOSFET due to scattering effects such as surface roughness scattering, phonon scattering, coulombic scattering from the interface, and bulk charge impurity scattering [2]. Furthermore, there is an increase in gate oxide current leakage when the thickness of the gate oxide layer is reduced. In contrast, in the CNTFET, we do not observe any such side effects. Instead, it performs better due to the ballistic transport of charge carriers for smaller channels and gate lengths [3].

Furthermore, CNTFETs also have good dielectric properties, which can carry large currents in smaller volumes, increasing the current mobility. SCE and scattering mechanisms do not affect CNTFETs. CNTFETs look promising in overcoming the challenges faced by MOS transistors in reducing the size of transistors. Nevertheless, it is still challenging to fabricate CNTFETs and requires extensive research to optimize the parameters to make commercial circuits available in the market. The current mobility, dielectric, and conductivity are highly influenced by the change in parameters of CNT devices. Physical parameters like chirality, channel length, diameter, pitch, gate length, gate width, oxide thickness, supply voltage, and number of tubes influence the performance of CNTFET [4,5].

Different optimization schemes and models for CNTFET are proposed to overcome the effects of parasitic capacitances and obtain good-performing CNT-based transistors [6,7,8,9]. Furthermore, CNT-based transistor devices show minor differences in characteristics when multiple transistors exist in circuits with different arrangements. One of the most critical parameters that affect CNTFET's behaviour is the chirality of the carbon nanotube. In simpler terms, chirality defines the length and the angle at which the graphene sheet is cut to be rolled up in a Carbon Nano Tube. Chirality comprises of two components, the chiral vector, defined as Ch, and the chiral angle, defined as Θ. Based on the chiral vector, a CNT can behave either as a metallic or semiconducting CNT. The CNT diameter is also critical, as it determines the bandgap, affecting the electrical conductivity and threshold voltage for CNTFETs [10].

There are mainly three kinds of CNTFETs depending on the mechanism, SB-CNTFET (Schottky Barrier CNTFET), Partially Gated (PG-CNTFET), and MOSFET like CNTFET. SB-CNTFET incorporates a planar carbon nanotube connecting the metal source and drain. This connection between metal contacts and carbon nanotubes creates a Schottky barrier at the point of intersection. While MOSFET-like CNTs are four-terminal transistors, partial CNTs across the transistor's channel, source, and drain are heavily doped semiconductors (P-type or N-type). The mechanism of this device is like traditional four-terminal MOS transistors. The MOSFET-like transistors are more advantageous over the Schottky barrier CNTFETs such as low leakage currents due to the absence of the Schottky barrier, unipolar characteristics, higher conductivity, and current capacity to reduction in thickness of the potential barrier [11]. Thus, in this research, we will simulate the behaviour and compare the performance of MOSFET like CNTFET with CMOS transistors.

This paper describes CNTFET behavior by varying various parameters and comparing the results with traditional MOSFET technology. Characteristics such as delay, leakage current, supply voltage, and average power will be discussed for basic logic gates that can be used to make combinational circuits. For changing the parameters of CNTFETs, some measures must be considered as the change in one parameter also changes the other related parameters. An inappropriate change in the parameter value may result in incorrect functionality and behavior of the model, leading to false simulation results. Stanford University designed one of the most accurate models after experimenting with the properties of CNTs at the quantum level [12]. We have used this model of CNTFET to compare the performance of CNTFET devices with CMOS devices.

Here are some default parameters shown in Table 1, used in the CNTFET Stanford model that can be optimized for better propagation delay, power, and leakage current results. For observing the impact and optimization of CNTFET, we considered changing parameters such as Pitch, chirality, dielectric constant, number of tubes, and T_{OX}. Pitch is the distance between two adjacent tubes in CNFET, and T_{OX} is the thickness of top gate dielectric material, while K_{OX} is the dielectric constant, subject to the material used in CNTFET. We randomly varied these parameters for the experiment and observed their effect on power consumption. The dielectric material enhances CNTFET's molecular properties and is used as a gate dielectric [13]. Different materials have been considered for CNTFET, such as SiO_2, HfO_2, TiO_2, etc.; all these materials have a different dielectric constant value.

Table 1. Default parameters for CNTFET

Parameter	Description	Default Value
L_{CH}	Channel length	32.0 nm
L_{GEFF} (L_{CEFF})	The mean free path in the intrinsic CNT channel region	200.0 nm
L_{SS} (L_{SD})	The length of doped CNT source-side	32.0 nm
L_{DD}	The length of doped CNT drain-side	32.0 nm
E_{FI} (E_{FO})	The Fermi level of the doped S/D tube	0.6 eV
K_{GATE} (K_{OX})	The dielectric constant of the high-k top gate dielectric	16.0
T_{OX}	The thickness of high-k top gate dielectric material	4.0 nm
C_{SUB}	The coupling capacitance between the channel region and substrate	20.0 pF/m
Pitch	The distance between the centers of two adjacent CNTs	20.0 nm
Chirality (n,m)	Chiral Vector	(19,0)
sub_pitch (W_{GATE})	Sub-lithographic pitch (Gate of width)	6.4 nm
Tubes	Number of tubes in one device	1

3. CNTFET Optimization

For optimization of CNTFET in terms of delay, static power, and dynamic power, we have changed one parameter of CNTFET at a time and recorded the performance for each parameter. For all these parameters, different values are recorded for three logical gates. All simulations are carried out at V_{DD} = 0.9V using H-spice. The parameters we considered for optimization of CNTFET were Chirality, Pitch, number of tubes, and dielectric constant K_{OX} of CNTFET. In the end, we have calculated the PDP for CNTFET as it is considered the best measure to check the performance of any transistor. We have also compared the optimized value of CNTFET with traditional transistors.

3.1 *Delay Optimization for CNTFET*

Delay time and switching speed are essential parameters for any transistor to improve the performance of electronic circuits. Propagation delay in transistors is the switching speed or time that a transistor takes to change the output signal to move from high to low or vice-versa with a change in the input signal. Several factors such as contact resistance, conductance, channel mobility, and reduced drain-induced barrier lowering affect propagation delay in transistors. In CNT, the configuration of connecting tubes can vary the conductance resulting in a change in the contact resistance; this can improve the switching speed and propagation delay in CNTFET. We have simulated the CNFET standard 32nm model and optimized the parameters to observe the effect of delay with change in parameters. The propagation delay of MOSFET shown in Table 2 is also calculated using H-Spice to compare its performance with optimized CNTFET. Propagation delay for CNTFET by varying parameters is shown in Tables 3–7. Lastly, after calculating the delay for different combinations of parameter values, we have come up with the optimized CNTFET parameters that give the minimum delay in Table 8.

Table 2. MOSFET Propagation Delay

Parameter	MOSFET Gate/Delay (E-11s)		
	NAND	NOR	NOT
T_{PHL}	4.747	2.289	2.292
T_{PLH}	1.102	5.281	1.986

Table 3. CNTFET Propagation Delay with Respect to Chirality

Chirality (n,m)	CNTFET Gate/Delay (E-11s)					
	NAND		NOR		NOT	
	T_{phl}	T_{plh}	T_{phl}	T_{plh}	T_{phl}	T_{plh}
13	48.47	6.75	2.854	6.117	2.974	2.968
19	14.27	1.558	1.38	2.822	1.398	1.396
25	8.897	1.441	1.067	2.14	1.087	1.054
27	9.510	1.565	1.032	2.043	1.05	1.008
38	17.11	1.281	0.89	1.73	0.917	0.866

Table 4. CNTFET Propagation Delay with Respect to Number of Tubes

No. of Tubes	CNTFET Gate/Delay (E-11s)					
	NAND		NOR		NOT	
	T_{phl}	T_{plh}	T_{phl}	T_{plh}	T_{phl}	T_{plh}
3	14.27	1.558	1.38	2.822	1.398	1.396
6	8.772	0.755	0.553	0.998	0.574	0.553
9	6.228	0.598	0.423	0.756	0.456	0.437
12	4.869	0.532	0.345	0.67	0.3825	0.3663

Table 5. CNTFET Propagation Delay with Respect to Pitch

Pitch (in nm)	CNTFET Gate/Delay (E-11s)					
	NAND		NOR		NOT	
	T_{phl}	T_{plh}	T_{phl}	T_{plh}	T_{phl}	T_{plh}
10	8.39	0.62	0.356	0.674	0.3902	0.3783
15	5.882	0.547	0.348	0.671	0.3847	0.3696
20	14.27	1.558	1.38	2.822	1.398	1.396
25	4.505	0.591	0.344	0.67	0.3815	0.3647

Table 6. CNTFET Propagation Delay with Respect to K_{OX}

K_{OX}	CNTFET Gate/Delay (E-11s)					
	NAND		NOR		NOT	
	T_{phl}	T_{plh}	T_{phl}	T_{plh}	T_{phl}	T_{plh}
12	16.84	9.454	0.374	0.687	0.4037	0.3966
16	14.27	1.558	1.38	3.822	1.398	1.396
23	1.410	0.435	0.313	0.637	0.3608	0.3385
27	1.081	0.41	0.299	0.662	0.3522	0.3271

Table 7. CNTFET Propagation Delay with Respect to H_{OX}

H_{OX} (in nm)	CNTFET Gate/Delay (E-11s)					
	NAND		NOR		NOT	
	T_{phl}	T_{plh}	T_{phl}	T_{plh}	T_{phl}	T_{plh}
3	0.91	0.38	0.288	0.66	0.345	0.3145
4	14.27	1.558	1.38	2.822	1.398	1.396
5	1.29	0.445	0.309	0.664	0.3582	0.3355
6	1.554	0.46	0.317	0.665	0.3636	0.3415

Table 8. Optimized Parameter Values for Propagation Delay and Propagation Delay Value

Parameters	CNTFET Gate		
	NAND	NOR	NOT
Chirality (n,m)	(25,0)	(38,0)	(38,0)
No. of Tubes	12	12	12
Pitch (in nm)	25	25	25
K_{OX}	27	27	27
H_{OX} (in nm)	3	3	3
T_{PHL} (E-11s)	0.9428	0.2886	0.3450
T_{PLH} (E-11s)	0.4306	0.606	0.3145

3.2 *Power Optimization for CNTFET*

With advancement in processors and high-performance machines, the processors are expected to perform at higher speeds with low power. But increasing frequency for better performance comes with a challenge of power consumption which results into increase in device temperature. Due to the Short Channel Effect (SCE), the channel length in MOS transistors comes to a limit. With reduced effective channel length, there is also an increase in leakage current in MOS transistors. At the same time, CNTFET shows better performance with the decrease in size of channel length due to the ballistic transport of carriers. Moreover, shortening of channel length is not responsible for leakage current and SCE in CNTFET. In CNTFET, with the variation of different parameters such as chirality, diameter, and Pitch, there is a significant increase in transistor behavior. Increasing the value of the chiral vector or diameter reduces the bandgap, which increases the on-current of the transistor. But, in contrast, this also increases the leakage current in the off state for CNTFET [14]. The ambipolar transport and gate-induced drain leakage due to electron tunneling across the drain side are responsible for the leakage current in Schottky Barrier CNTFETs.

The vital parameter in lowering the leakage current is the threshold voltage, which is dependent on the energy gap (The gap between the Valence Band and the Conduction Band) of the semiconducting material. The chirality (Chiral vector) of PFET and NFET in CNT devices can have different values, and the difference in these values also affects the value of threshold voltage. This increases the high ON-Current but also increases the OFF-Leakage current [15,16]. But, as stated earlier, the design of CNTFET is complex, and its characteristics change effectively with changes in parameters such as channel length, diameter, pitch, chirality, and Tox (Oxide Thickness). So, to obtain the optimized CNTFET device that shows good performance in terms of dynamic power, we have simulated the design, and power for each parameter is calculated. MOSFET Dynamic power consumption is shown in Table 9, and CNTFET power consumption for varying parameters is shown in Tables 10–14. We have compared the dynamic power consumption values in CMOS transistors with unoptimized CNTFET. Afterward, we have gone through several experiments by changing the parameters to get superior performance in CNTFET. The results are summarized in Table 15.

Table 9. MOSFET Dynamic Power Consumption

MOSFET Channel Length	Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
32 nm	0.1754	0.1201	0.1441

Table 10. CNTFET Dynamic Power Consumption with Respect to Chirality

Chirality (n,m)	CNTFET Gate/Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
13,0	0.5615	0.7635	1.003
19,0	0.5654	0.4685	2.358
25,0	0.5505	0.3299	0.895
27,0	0.4701	0.2482	0.0195
38,0	0.4842	0.2423	0.723

Table 11. CNTFET Dynamic Power Consumption with Respect to Number of Tubes

No. of Tubes	CNTFET Gate/Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
3	0.5654	0.4685	2.358
6	0.05733	0.4862	5.096
9	0.5571	0.7262	2.103
12	1.175	1.535	2.114

Table 12. CNTFET Dynamic Power Consumption with Respect to Pitch

Pitch (in nm)	CNTFET Gate/Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
10	0.3117	1.477	2.339
15	0.7213	1.522	0.3726
20	0.5654	0.4685	2.358
25	0.1150	1.538	6.345

Table 13. CNTFET Dynamic Power Consumption with Respect to K_{OX}

K_{OX}	CNTFET Gate/Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
12	0.4777	1.450	1.247
16	0.5654	0.4685	2.358
23	1.052	1.362	9.533
27	3.602	1.476	9.707

Table 14. CNTFET Dynamic Power Consumption with Respect to H_{OX}

H_{OX} (in nm)	CNTFET Gate/Dynamic Power Consumption (in nW)		
	NAND	NOR	NOT
3	4.042	1.379	5.992
4	0.5654	0.4685	2.358
5	2.839	1.484	9.331
6	2.170	1.488	1.076

Table 15. Optimized Parameter Values for Dynamic Power and Dynamic Power Value

Parameters	CNTFET Gate		
	NAND	NOR	NOT
Chirality (n,m)	27,0	38,0	27,0
Pitch (in nm)	25	20	20
No. of Tubes	6	3	3
K_{OX}	12	16	16
H_{OX} (in nm)	4	4	4
Dynamic Power (in nW)	0.05733	0.2423	0.0195

3.3 *Power-Delay Product*

Power delay product (PDP) is considered the best measure to evaluate the performance of the device, considering both the power consumption and propagation delay of transistors [17]. We have used the delay and power results to get the value of PDP, and the best combination of parameters that result in minimum PDP can be used to make the combinational circuit. Lastly, optimized CNTFET is compared with the unoptimized model and traditional MOSFET transistors. As shown in Tables 16–21, we observed the effect of Chirality, Oxide thickness, dielectric constant, pitch, and the number of tubes on PDP. The lowest PDP for NAND, NOR, and NOT gates are recorded and compared to MOSFET devices. As PDP, accounts for switching time and power consumption in switching, that is considering the speed and performance of the device, it is considered one of the best measures to evaluate device performance. We can see, pitch, the number of tubes, and chirality have a significant impact on PDP compared to dielectric material thickness and constant.

Table 16. MOSFET Power Delay Product

MOSFET Power Delay Product (in E-20 J)		
NAND	NOR	NOT
0.5129573	0.454579	0.30823

Table 17. CNTFET Power Delay Product with Respect to Chirality

Chirality (n,m)	Power Delay Product (in E-20J)		
	NAND	NOR	NOT
13,0	15.503015	3.424679	2.979913
19,0	4.4745756	0.984319	3.294126
25,0	2.8455345	0.528995	0.958098
27,0	2.60317875	0.381608	0.020066
38,0	4.4524611	0.317413	0.644555

Table 18. CNTFET Power Delay Product with Respect to Number of Tubes

No. of Tubes	Power Delay Product (in E-20J)		
	NAND	NOR	NOT
3	4.4745756	0.984319	3.294126
6	0.273091455	0.377048	2.871596
9	1.9013823	0.428095	0.93899
12	3.1730875	0.779013	0.791482

Table 19. CNTFET Power Delay Product with Respect to Pitch

Pitch (in nm)	Power Delay Product (in E-20J)		
	NAND	NOR	NOT
10	1.4042085	0.760655	0.898761
15	2.31861885	0.775459	0.140526
20	4.4745756	0.984319	3.294126
25	0.29302	0.779766	2.36732

Table 20. CNTFET Power Delay Product with Respect to K_{OX}

K_{OX}	Power Delay Product (in E-20J)		
	NAND	NOR	NOT
12	6.2803219	0.769225	0.498987
16	4.4745756	0.984319	3.294126
23	0.97047	0.64695	3.333213
27	2.685291	0.709218	3.296983

Table 21. CNTFET Power Delay Product with Respect to H_{OX}

H_{OX} (in nm)	Power Delay Product (in E-20J)		
	NAND	NOR	NOT
3	2.60709	0.653646	1.975862
4	4.4745756	0.984319	3.294126
5	2.4628325	0.721966	3.236457
6	2.18519	0.730608	0.379344

After going through all the extensive simulations of power consumption and delay for these three logic gates and calculating the PDP based on the results, we have the optimized parameters with the lowest PDP value for all three gates shown in Table 22.

The following Figures 1–5 depict the variation in PDP by changing various CNTFET parameters for NAND, NOR and NOT gate.

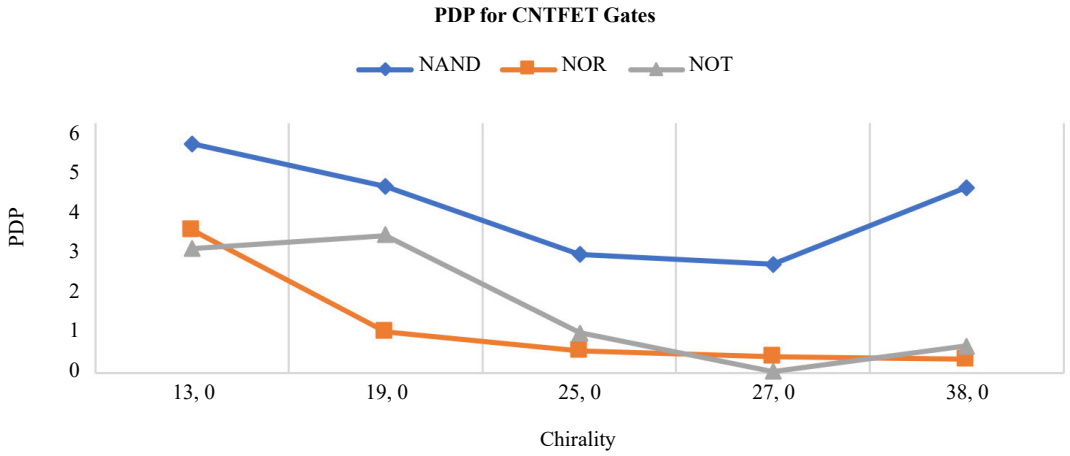

Figure 1. Variation in PDP with respect to Chirality

We can see a decreasing trend in PDP as we increase the chirality of the CNTs.

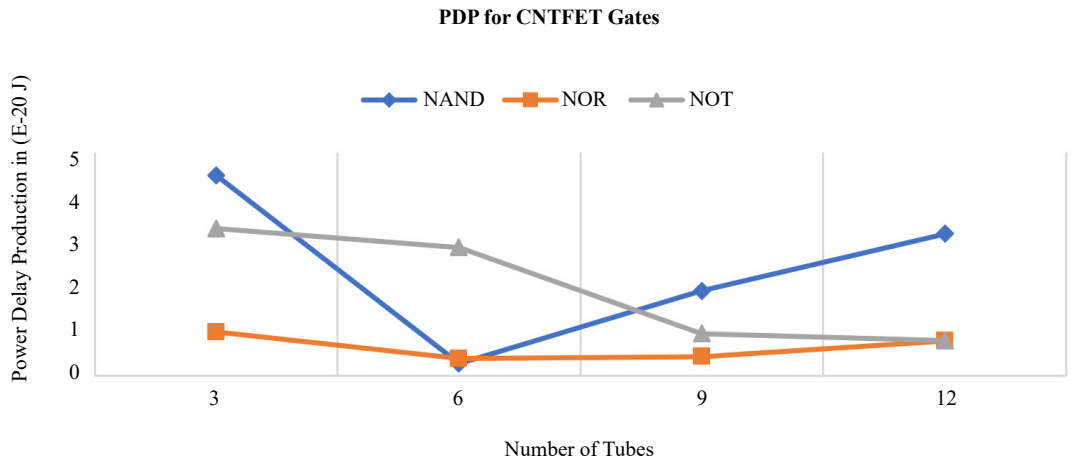

Figure 2. Variation in PDP with respect to number of Tubes

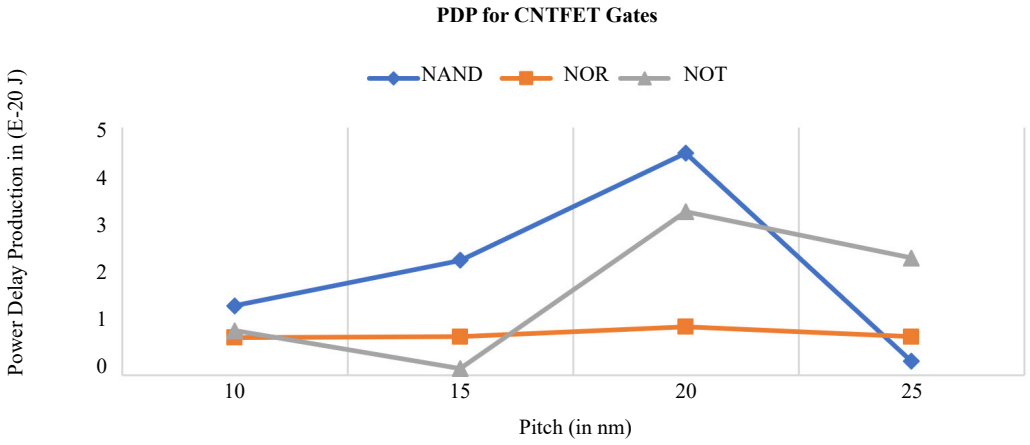

Figure 3. Variation in PDP with respect to Pitch

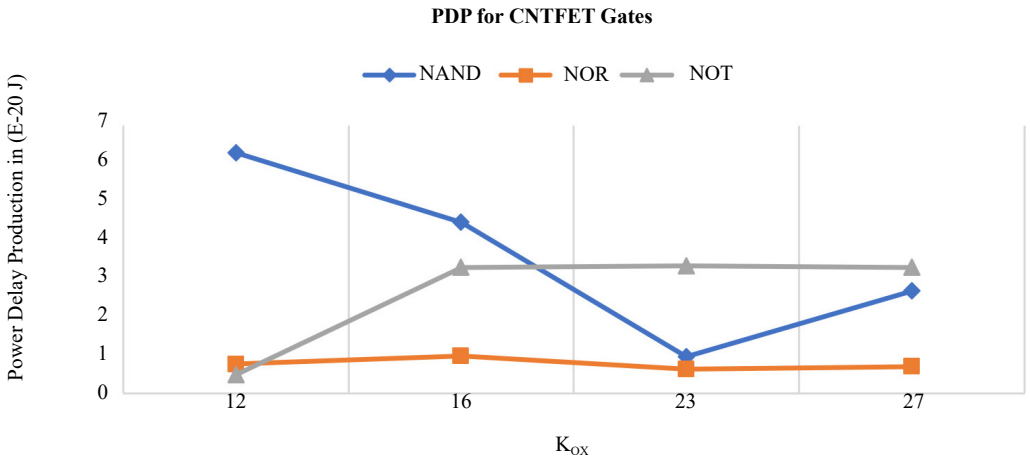

Figure 4. Variation in PDP with respect to K_{OX}

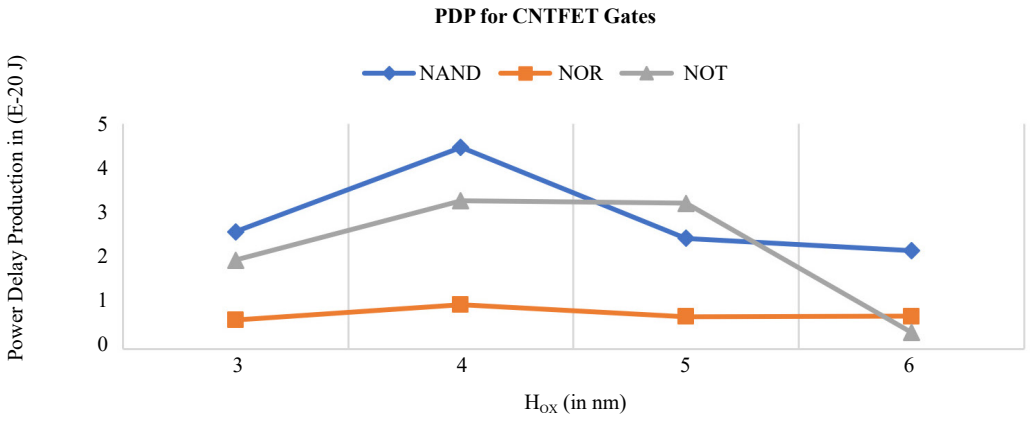

Figure 5. Variation in PDP with respect to number of Tubes

Table 22. Parameters for Optimized Power Delay Product for CNTFET

GATE	NAND	NOR	NOT
Parameter	No. of Tubes: 6	Chirality(n,m): (38,0)	Chirality(n,m): (27,0)
PDP (in E-20 J)	0.2730	0.317	0.020066

4. Conclusion and Future Works

We have done intensive simulations on basic logic gates derived from CNTFET and MOSFET transistors to evaluate the performance of evolving technology CNT-based transistors to keep up with Moore's law. The CNTFET devices without optimization show comparatively lower performance than traditional silicon based MOSFET transistors. But, after optimizing the parameters namely Chirality, Oxide thickness, dielectric constant, Pitch, and the number of tubes with respect to propagation delay and power dissipation, we get a better performing device with CNTFET over MOSFET.

The CNTFET transistors have many advantages over silicon transistors, but still, it is challenging to make IC derived of CNTFET transistors. We have calculated the optimum parameters for CNTFET-based logic gates for best performance. Also, simulation on identical chirality for both P and N-type CNTFET is performed, but in upcoming research, we will also consider dual chirality to optimize the power consumption in CNTFET devices. The optimum parameters for logic gates we obtained in this research might change for the combinational circuit, so we will be conducting research based on different combinational circuits to observe the behavior of transistors. Furthermore, we will evaluate the performance of other evolving technology such as FinFET, Silicon-On-Insulator Field Effect transistors (SOIFET), and GNRFET based transistors.

Conflict of Interest

There is no conflict of interest for this study.

References

[1] Choi, D.S.; Mallick, G.; Karna, S.P. Effect of low-energy electron beam irradiation on the current-voltage characteristics of single-walled carbon nanotube field effect transistors. In Proceedings of 2017 IEEE 17th International Conference on Nanotechnology (IEEE-NANO), Pittsburgh, PA, USA, 25–28 July 2017. https://doi.org/10.1109/nano.2017.8117335.

[2] Chaudhry, A.; Sangwan, S.; and Roy, J.N. Mobility Models for Unstrained and Strained Silicon MOSFETS: A Review. *Contemp. Eng. Sci.* **2011**, *4,* 229–247.

[3] Karimi, A.; Rezai, A. A Design Methodology to Optimize the Device Performance in CNTFET. *ECS J. Solid State Sci. Technol.* **2017**, *6,* M97–M102, https://doi.org/10.1149/2.0181708jss.

[4] Jooq, M.K.Q.; Mir, A.; Mirzakuchaki, S.; Farmani, A. Semi-analytical modeling of high performance nano-scale complementary logic gates utilizing ballistic carbon nanotube transistors. *Phys. E: Low-dimensional Syst. Nanostructures* **2018**, *104,* 286–296, https://doi.org/10.1016/j.physe.2018.08.008.

[5] Hadi, M.F.A.; Hussin, H.; Muhamad, M.; Soin, N.; Wahab, Y.A. Effects of Different Oxide Thicknesses on the Characteristics of CNTFET. In Proceedings of 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM), Kuala Lumpur, Malaysia, 2–4 August 2021. https://doi.org/10.1109/rsm52397.2021.9511584.

[6] Cho, G.; Lombradi, F.; Kim, Y-B. Modeling Undeposited CNTsfor CNTFET Operation. *IEEE Trans. Device Mater. Reliab.* **2011**, *11,* 263–272, https://doi.org/10.1109/TDMR.2011.2123896.

[7] Patil, N.; Deng, J.; Lin, A.; Wong, H.-S.P.; Mitra, S. Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **2008**, *27,* 1725–1736, https://doi.org/10.1109/tcad.2008.2003278.

[8] Pregaldiny, F.; Lallement, C.; Kammerer, J-B. Design-oriented compact models for CNTFETs. In Proceedings of International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006.

Tunis, Tunisia, 5–7 September 2006. https://doi.org/10.1109/DTIS.2006.1708732.
[9] Hussin, H.; Abdul Hadi M.F.; Soin, N. Optimizing CNTFET design parameters using Taguchi method for high performance and low power applications. *J. Eng. Res.* **2022**, https://doi.org/10.36909/jer.14155.
[10] Hadi, M.F.A.; Hussin, H.; Soin, N. The Impact of Variation in Diameter and Dielectric Materials of the CNT Field-Effect Transistor. *ECS J. Solid State Sci.* Technol. **2022**, *11,* 023002, https://doi.org/10.1149/2162-8777/ac4ffc.
[11] Dang, T.; Anghel, L.; Leveugle, R. CNTFET basics and simulation. In Proceedings of International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. Tunis, Tunisia, 5–7 September 2006. https://doi.org/10.1109/dtis.2006.1708731.
[12] Stanford CNT Transistor Model. Available online: https://nano.stanford.edu/downloads/stanford-cnfet-model/stanford-cnfet-model-hspice (accessed on 1 June2019)
[13] Kumar M.; Ubhi, J.S. Design and analysis of CNTFET based 10T SRAM for high performance at nanoscale. *Int. J. Circuit Theory Appl.* **2019**, *47,* 1775–1785, https://doi.org/10.1002/cta.2696.
[14] Zhang, J.; Lin, A.; Patil, N.; Wei, H.; Wei, L.; Wong, H.-S.P.; Mitra, S. Carbon Nanotube Robust Digital VLSI. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **2012**, *31,* 453–471, https://doi.org/10.1109/tcad.2012.2187527.
[15] Xu, L.; Qiu, C.; Peng, L.-M.; Zhang, Z. Suppression of leakage current in carbon nanotube field-effect transistors. *Nano Res.* **2020**, *14,* 976–981, https://doi.org/10.1007/s12274-020-3135-8.
[16] Sayed, S.I.; Abutaleb, M.M.; Nossair, Z. Optimization of CNFET Parameters for High Performance Digital Circuits. *Adv. Mater. Sci. Eng*. **2016**, *2016,* 1–9, https://doi.org/10.1155/2016/6303725.
[17] Han, Z. The power-delay product and its implication to CMOS Inverter. *J. Physics: Conf. Ser.* **2021**, *1754,* 012131, https://doi.org/10.1088/1742-6596/1754/1/012131.