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Article

On-Wafer Drain Current Variability in GaN MIS-HEMT on 200-mm Silicon Substrates

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Abstract: In this study, a detailed on-wafer (or global) variability analysis of drain current characteristics of GaN MIS-HEMT devices grown on 200 mm silicon substrate is conducted. For the first time to our knowledge, the on-wafer variability sources in GaN technologies due to the manufacturing process are investigated by combining experimental data and analytical variability modeling. The key parameters which affect the variability are oxide the interface charge fluctuations, the mobility fluctuations, the gate oxide thickness and/or the gate area variations and the access resistance fluctuations in the contact as well as in the 2DEG regions (source and drain sides). Due the specificity of GaN MIS HEMT device engineering process, we show that their variability performances are not, for the time being, comparable to the state-of-the art silicon CMOS technologies, and this can be valuable for reliable improvement and optimization of GaN technology fabrication process. This study has been verified over a large range of channel gate lengths for three normally-off GaN MIS-HEMT wafers and having different gate process flows.

Keywords: on-wafer variability, modeling, GaN MIS-HEMT, normally-off, mobility, source-drain access resistance

1. Introduction

Heterojunction device-based AlGaN/GaN high electron mobility transistors (HEMTs) have attracted a lot of attention in the last decade in power electronics and RF applications [1]. Their performances require a high breakdown voltage, high electron mobility at AlGaN/GaN interface, low ON-resistance, high operating temperature and for RF application, a high field saturation speed and low parasitic capacity [2–6]. As the manufacturing fabrication volumes of GaN HEMT devices increase, it is necessary to analyse the variability of transistor electrical performances due to the fabrication process variation. Such on-wafer or global variability studies are useful for development and process engineer. Development engineers can use this methodology to analyse the sensitivity of process variations on electrical performance and tune the manufacturing process accordingly. Design of a significant number of GaN components on the same wafer are generally done with an objective to realize the same performance. In the reality, they have different electrical properties which depend on their fabrication process and their position on the same wafer (200 mm in this work) or from wafer to wafer. However, following the progressive miniaturization of GaN devices for power electronics or RF-circuit, the variability performances must be considered to obtain a reliable manufacturing process. For silicon technology, Mizuno et al. [7] have shown experimentally that the V_{th} fluctuations depend on the channel length and the gate oxide thickness. However, they demonstrated that V_{th} fluctuations are directly correlated with the dopant number

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fluctuations in the channel region. Various methodologies to analyse local and global variability have been proposed [8–11], but this is less the case for GaN devices.

In previous studies [12], a statistical characterization and statistical extraction of electrical parameters was presented for the same type of GaN MIS-HEMT devices. We apply here, for the first time, a methodology generally used in silicon technologies to analyse the variability of intrinsic electrical parameters such as drain current as well as the access resistance, gain parameter and threshold voltage [9]. Thus, the aim of this study is to employ this approach to analyse the on-wafer variability on I_d-V_g characteristics of the GaN MIS-HEMT devices with recessed gate, and to discriminate the contribution of the active channel and of the source-drain access resistances. This will be useful to improve the manufacturing process of GaN MIS-HEMT technologies. We will first describe the studied wafers, device architecture and electrical characterization protocol. Next, we will recall electrical characterization of GaN MIS-HEMT and their influence on the effective gate length of the HEMT devices [5,12]. A global variability analysis is then performed between different gate length and different wafers. All experimental data are well fitted by the variability models which were used previously in silicon technologies. Finally, we will compare the parameter variability extracted in this work with those from best silicon technologies.

2. Devices and Experiment Methods

Electrical measurements were performed on different wafers processed with GaN MIS-HEMT technology with a fully recess depth (RD>t_{AlGaN}) to ensure normally-off mode (Figure 1a). GaN epitaxy is performed by Metal-Organic-Chemical Vapor Deposition (MOCVD), on 200 mm diameter silicon (111) substrates. The structure is composed of an AlN nucleation layer, an AlGaN based buffer, C-doped GaN buffer layers to ensure a high breakdown voltage, then an unintentionally doped (UID) GaN channel in which a back-barrier (doped layer) can be inserted. The total epitaxy layer thickness is about 4 µm. The piezoelectric effect to form the 2D electron gas (2DEG) is obtained with the growth of AlN spacer and an $Al_xGa_{1-x}N$ barrier layer on top of the GaN channel layer, followed by in-situ deposition of a passivation layer [13,14].

The fully recessed Metal-Insulator Semiconductor (MIS) HEMT are processed by dry etching of AlGaN and UID-GaN layers in the gate area and Al_2O_3 gate oxide are processed by Atomic Layer Deposition (ALD) or by plasma enhanced atomic layer deposition PEALD in which AlN oxide spacer can be inserted (Figure 1a and 1b) to give an equivalent gate oxide thickness Al_2O_3/AlN [15]. The GaN channel in the recessed region, under the gate oxide presents a particular shape formed of the gate sidewalls with a specific angle, the gate corners and the gate bottom. Figure 1c shows a cross sectional TEM of the fully recessed MIS gate region with different typical interfaces.

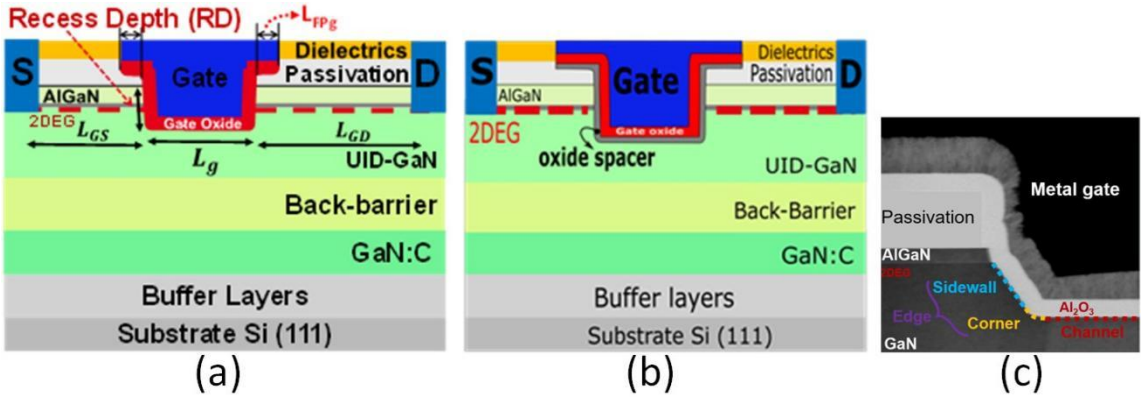

Figure 1. Schematic cross section of GaN/Si MIS-HEMT stack (a) without and (b) with oxide spacer and (c) TEM Cross-sectional image of the recessed MIS gate without oxide spacer with different typical interfaces.

The test structures reported in this study were fabricated using three different process flows. The differences consist mainly in the fabrication steps such as optimization of the ohmic contacts process, the gate etching process and MIS gate depositions recipe. Wafers 1, 2 and 3 correspond to two different recess depths, a shallow gate recess (RD1) and a deep gate recess (RD2) [RD1<RD2]. Wafers 2 and 3 have approximatively the same recess depth RD2. Notice that, the etching process on the gate region can affect the electrostatics control of channel layer in this region, but the source-drain access resistance remains the same. The source and drain are composed of metallic Ohmic contacts (Ti/AlCu) connected to the 2D electron gas (2DEG) formed at the

AlGaN/GaN interface. The symmetrical tested devices were T-metal gate only with same gate field plate length on the source and drain sides such as L_{FPg} = 0.25 µm. The different gate lengths for wafers #1 and #2 (RD1 and RD2, respectively) varying from 0.5 to 10 µm and with the same width (W = 100 µm), and for wafer #3, the gate lengths varying from 0.25 µm, 2 µm and 200 µm width (Table 1). The source-gate and drain-gate lengths are equal ($L_{gs} = L_{gd}$ = 2 µm). The I_d-V_g transfer characteristics were measured in linear regime ($V_d < kT/q$) using an B1500 Semiconductor Device Analyser. The C_{gc}-V_g characteristics were measured by split CV method owing to an HP 4284 LCR meter at a frequency of 10 kHz for short channel and 1 kHz for long channel to avoid channel response time and trap response effects, specific to GaN MIS-HEMT devices.

Table 1. Key parameters for wafers #1, #2 and #3

Parameters	Wafer #1	Wafer #2	Wafer #3
L_g range [µm]	0.5 to 50	0.5 to 50	0.25 to 2
W [µm]	100	100	200
Effective oxide	Al_2O_3	Al_2O_3	Al_2O_3/AlN
L_{FPg} [µm]	0.25	0.25	0.25
$L_{gs} = L_{gd}$ [µm]	2	2	2

The GaN MIS-HEMTs parameters extraction was carried out using the Y-function based protocol, which allowed to evaluate the source-drain access resistance values and to remove their influence on the I_d-V_g transfer characteristics and mobility. This method was originally developed for Si-MOSFETs [16] and recently applied and validated on MIS-HEMT GaN devices at room temperature [12,17], then, at different temperatures down to deep cryogenic temperatures [18]. The Y-function is defined from drain current I_d and transconductance g_m by:

$$Y(V_g) = I_d(V_g) / \sqrt{g_m(V_g)} \tag{1}$$

In strong inversion, the Y-function has a linear behaviour such as $Y(V_g) \approx \sqrt{\beta \cdot V_d}(V_g - V_{th})$, where $\beta = WC_{ox}\mu_0/L$ is the transconductance parameter, C_{ox} is the intrinsic gate oxide capacitance, μ_0 is the low field mobility and V_{th} the threshold voltage without source-drain access resistance effect. The source-drain access resistance is then extracted on each HEMT device, in linear operation and from the asymptotic behaviour parallel to the x axis (plateau) of the quantity defined below plotted in the strong inversion region.

$$R_{SD} \approx \frac{V_d}{I_d(V_g)} - \frac{1}{\beta \cdot (V_g - V_{th})} \tag{2}$$

3. Results and Discussion

3.1 *Transfer Characteristics and Electrical Parameters*

Figure 2 shows typical statistical set of drain current $I_d(V_g)$ characteristics as a function of the gate voltage obtained on 25 devices of wafer #1 and wafer #2 at 25°C. The dispersion of the characteristics observed in Figure 2a in strong inversion regime is known to result from the degraded source and drain ohmic contact resistance [12].

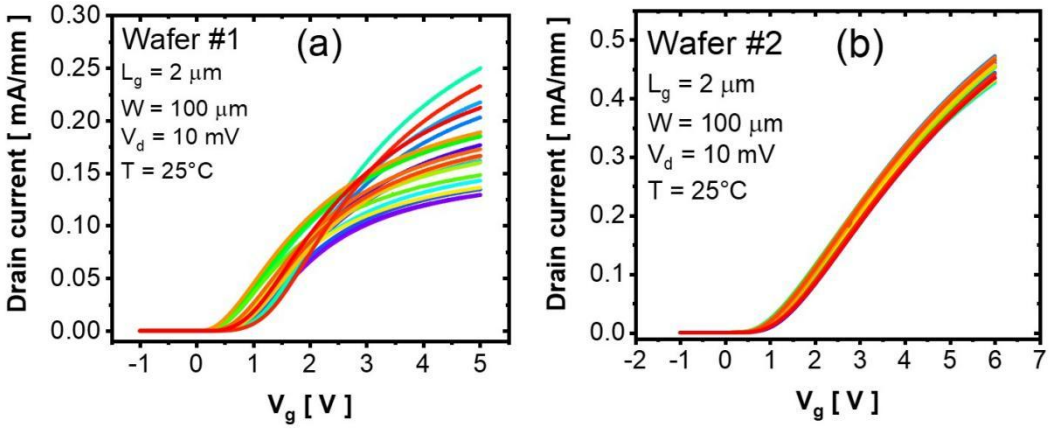

Figure 2. Typical set of $I_d(V_g)$ characteristics measured on GaN MIS-HEMT devices for (a) wafer #1 and (b) wafer #2 (Al_2O_3/GaN interface).

Figure 3 shows different values of source-drain access resistance extracted from Eq. (2). A higher and more distributed source-drain access resistance mean values are found on Wafer #1 (around 45 Ω·*mm*, Figure 3a) but, small and less distributed for wafer #2 (around 6 Ω·*mm*, Figure 3b) and wafer #3 (around 5 Ω·*mm*, Figure 3c) This clearly shows an improvement in the quality of the ohmic contacts for this GaN process flow.

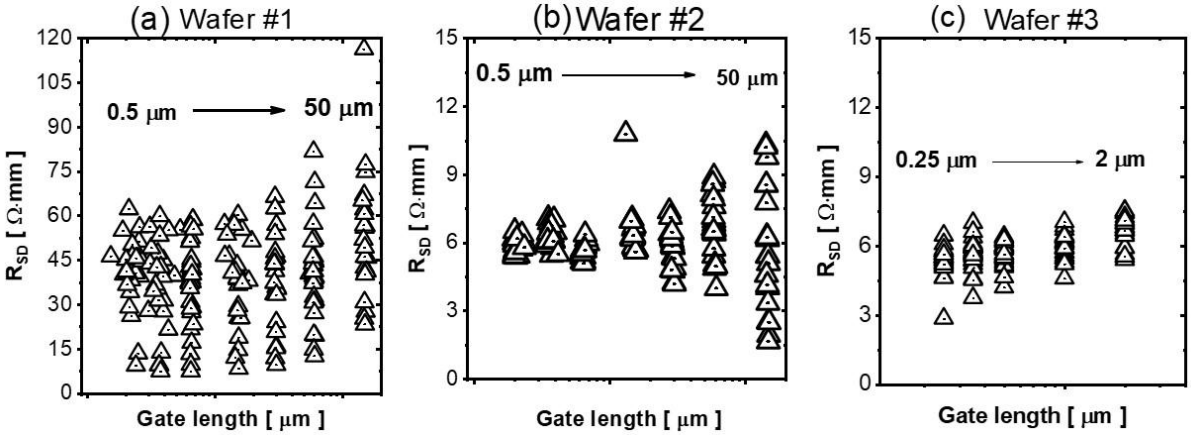

Figure 3. Variations of source-drain access resistance values R_{SD} extracted by Y-function method obtained on GaN/Si MIS-HEMT devices for various gate lengths L_g from 0.5, to 50 µm for wafer #1 and #2 (V_d = 10 mV, W = 100 µm and T = 25°C). and from 0.25 to 2 µm for wafer #3 (V_d = 20 mV, W = 200 µm and T = 25°C).

Using source-drain access resistance R_{SD} values extracted previously from Eq. (2), the $I_d(V_g)$ characteristics and effective mobility $\mu_{split}(N_{ch})$ can be corrected according to the Eqs (3) and (4), respectively:

$$I_{d\_Corr}(V_g) = I_d(V_g) \times \frac{1}{1 - \frac{I_d(V_g)}{V_d} \times R_{SD}} \tag{3}$$

$$\mu_{Corr}(N_{Ch}) = \mu_{split}(N_{Ch}) \cdot \frac{1}{1 - \frac{I_d(V_g)}{V_d} \times R_{SD}} \tag{4}$$

where $\mu_{split}(N_{ch}) = L \cdot I_d(V_g) / W \cdot V_d \cdot Q_{ch}(V_g)$ is the classical split-CV mobility, $Q_{ch} = q \cdot N_{ch}$ is the total channel charge obtained from the integration of C_{gc}-V_g characteristics.

Figure 4 shows the $I_d(V_g)$ characteristics of raw data for wafer 1 without (Figure 4a) and with (Figure 4b) source-drain series resistance correction in linear regime (V_d = 10 mV). The impact of source-drain access resistance R_{SD} can be clearly seen from the I_d-V_g characteristics of GaN MIS-HEMT devices for wafer #1 (see Figure 4a), where the curve dispersion is small in near-threshold region but huge in strong inversion region.

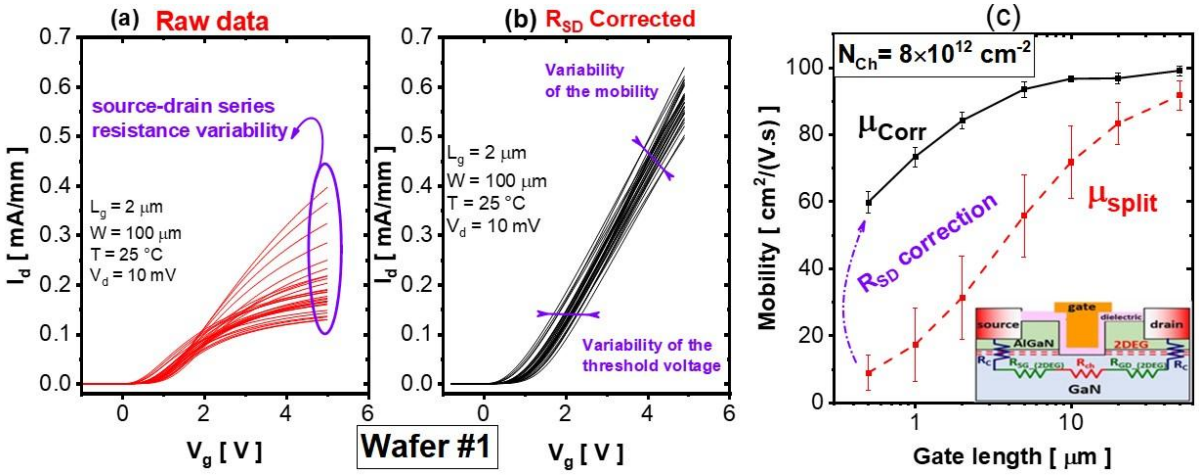

Figure 4. $I_d(V_g)$ characteristics without (a) and with (b) source-drain access resistance correction and (c) The Split CV mobility with μ_{Corr} and without μ_{split} source-drain access resistance effects obtained from Y-function method.

After source-drain access resistance effects removing, these dispersions are greatly reduced (see Figure 4b). The split-CV effective mobility variations with channel length obtained without and with source-drain access resistance are shown in Figure 4c. It also clearly confirms that the mobility value dispersion before correction is really due to the source-drain access resistance variations.

Moreover, the mean values of the drain current characteristics $I_d(V_g)$ in linear regime were fitted with Eq. (5).

$$I_d(V_g) = \frac{W}{L} \cdot \mu_{eff}(V_g) \cdot Q_{Ch}(V_g) \cdot V_d \tag{5}$$

where the channel charge Q_{ch} is computed from weak to strong inversion using Lambert compact model as,

$$Q_{Ch}(V_g) = C_{ox} n \frac{k_B T}{q} LW \left[\exp\left(q \frac{V_g - V_{th}}{n k_B T} \right) \right] \tag{6}$$

where k_BT/q is the thermal voltage, n is the ideality factor which can be obtained from the subthreshold slope, LW is the Lambert-W function [19], V_{th} is the threshold voltage and C_{ox} the intrinsic gate oxide capacitance. The effective mobility taking into account the influence of the source-drain access regions is given by Eq. (7),

$$\mu_{eff}(Q_{Ch}) = \frac{\mu_0}{1 + \theta_1 \left(\frac{Q_{Ch}}{C_{ox}} \right)} \tag{7}$$

where μ_0 is the low field mobility, $\theta_1 = \theta_0 + R_{SD} \cdot \beta$ is the first order mobility attenuation coefficients, θ_0 being the intrinsic first order mobility attenuation factor (around 0.03 V^{-1} here) and $\beta = \frac{W}{L} \cdot C_{ox} \cdot \mu_0$ the current gain factor.

Figures 5a and 5b show the best fit of typical drain current transfer characteristics I_d-V_g in linear regime for different wafers. The corresponding transconductance g_m-V_g and Y-V_g characteristics (experimental and modeling) are shown in Figure 5c and 5d, illustrating a larger maximum transconductance on wafer #3 and a larger slope of Y-function in strong inversion due to the higher mobility. Note that the Y-functions are almost identical for wafers #1 and #2 due to the same intrinsic mobility. However, we can see from Figure 5c a larger slope on normalised Y-function characteristics for wafer #3 as compared to wafer #1 and #2.

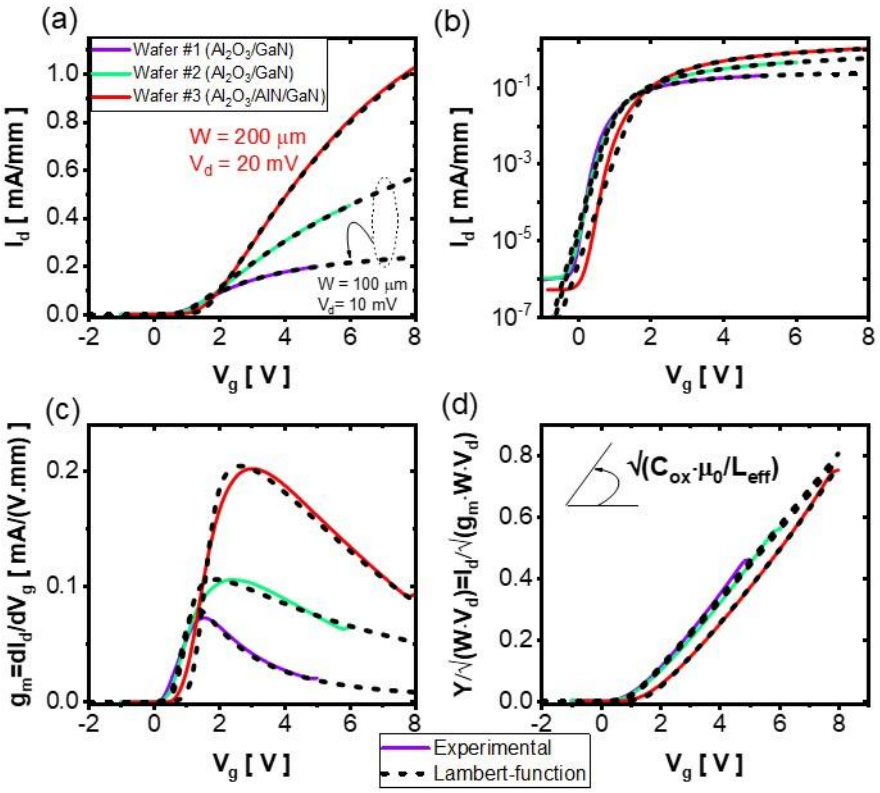

Figure 5. (a) and (b) Typical $I_d(V_g)$ characteristics experimental and modelled measured on GaN MIS-HEMT devices of wafer #1 and #2 (W = 100 µm, V_d = 10 mV) and #3 (W = 200 µm, V_d = 20 mV) at room temperature (T = 25°C) in linear and log scale respectively, (c) transconductance and (d) normalized Y-function characteristics.

Figure 6 shows the mean values of the intrinsic channel mobility characteristics $\mu_{eff}(N_{ch})$ for different wafers #1, #2 and #3 measured on GaN MIS-HEMT by split CV technique. We can see that, for wafers #1 and #2, we have the same mobility value for the Al_2O_3/GaN interface, whereas it is significantly improved for the Al_2O_3/AlN/GaN interface in wafer #3, due to the interposition of the AlN oxide spacer layer.

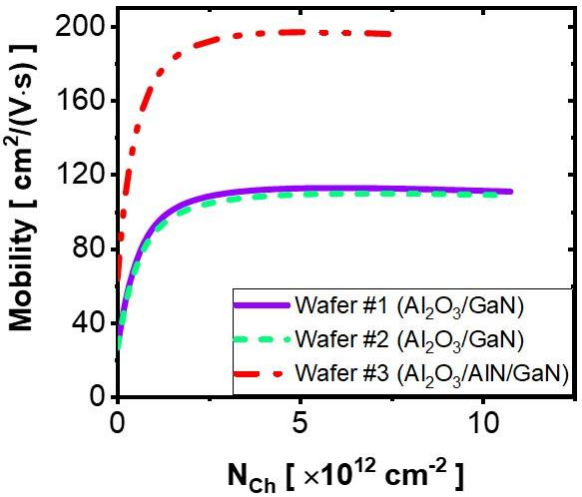

Figure 6. Effective mobility characteristics of free carriers measured on GaN MIS-HEMT devices for different wafers #1, #2 and #3.

3.2 *Drain current Global variability Methodology*

We have shown previously a statistical extraction methodology of intrinsic electrical parameter from the I_d-V_g curves [12]. This enabled us to show that it is possible to remove for each GaN MIS-HEMT device the source-drain access resistance effect on the intrinsic parameters of the active channel. In classical GaN technology study, these extracted parameters can be screened for devices placed in different regions all over the wafer or on different wafers. Here, we explored the global or on-wafer variability of the drain current and Y-

function characteristics measured on 200 mm GaN/Si wafers using, for the first time, the methodology that was originally developed for Si-MOSFETs based on the analysis of the drain current standard deviation characteristics as a function of gate voltage V_g.

The global variability of drain current $\Delta I_d/I_d$ is thus defined using the logarithmic difference as [9–11]:

$$\frac{\Delta I_d}{I_d} = ln(\frac{I_{d,i}}{I_{d,Mean}}) \tag{8}$$

where $I_{d,i}$ are the drain current of devices i and $I_{d,Mean}$ is the mean drain current of 25 devices (Figure 7a and 7b). Similarly to Eq. (8), we can also calculate the global variability of Y-function such as $\Delta Y/Y = ln(Y_i/Y_{Mean})$ .The corresponding global variability of the drain current $\Delta I_d/I_d$ measured from different GaN MIS-HEMT transistors on wafers #1, #2 and #3, respectively, are shown in Figure 7. It clearly indicates that, for wafer #3, up to 5 decades of dispersion of the drain current can be reached below threshold as compared to wafer #1, where it is about 4 decades, while for wafer #2 it can reach 1.5 decade (note that 2.3 on y axis corresponds to 1 decade of log 10 difference between $I_{d,Mean}$ and $I_{d,i}$).

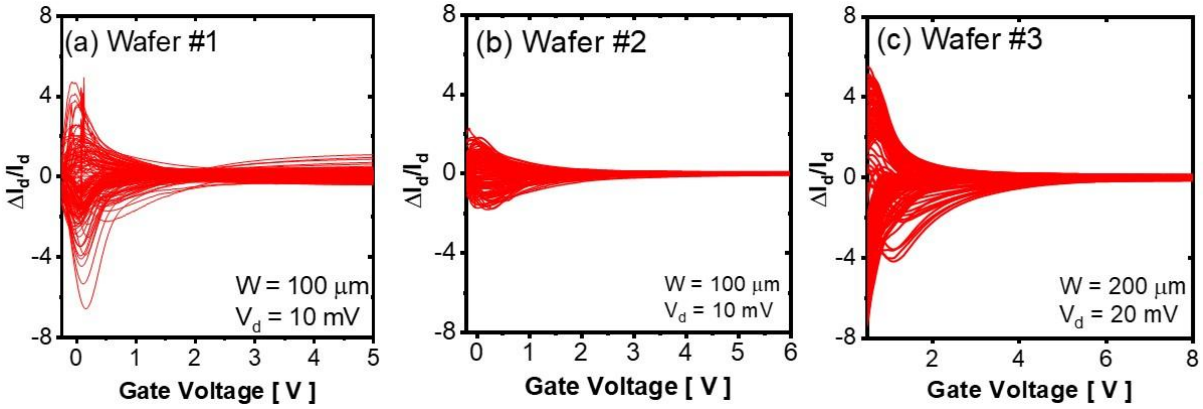

Figure 7. Variations of global variability $\Delta I_d/I_d$ versus gate voltage obtained from different GaN/Si MIS-HEMT of the different wafers (a) #1, (b) #2 et (c) #3.

For wafer #1, we observe an increase of the global drain current variability $\Delta I_d/I_d$ in strong inversion when the gate bias is increased (see Figure 7a), whereas the global variability on wafer #2 and #3 decreases or remains constant above threshold (see Figure 7b and 7c, respectively). This is because the drain current variability is dominated in strong inversion by the source-drain access resistance variability. This will be confirmed below by the standard deviation analysis.

To better quantify and analyse the variability of the drain current and the Y-function (defined in Eq. (1)), we can compute respectively the standard deviation associated to their global variability $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta Y/Y)$. To this end, following [9–11], a sensitivity analysis of the drain current function $I_d = f(V_{th}, \beta, R_{SD})$ and of the Y-function $Y = f(V_{th}, \beta)$ versus V_{th} , β and R_{SD} variables can be carried out as in Eqs (9) and (10), respectively. Consequently, as in silicon technology, it can be shown that $\sigma(\Delta I_d/I_d)$ and $\sigma(\Delta Y/Y)$ characteristics can be modelled with expressions given in Eqs (11) and (12) [9–11].

$$\frac{\sigma I_d}{I_d} = \frac{1}{I_d}\frac{\partial I_d}{\partial V_{th}}\sigma V_{th} + \frac{1}{I_d}\frac{\partial I_d}{\partial \beta}\sigma\beta + \frac{1}{I_d}\frac{\partial I_d}{\partial R_{SD}}\sigma R_{SD} \tag{9}$$

$$\frac{\sigma Y}{Y} = \frac{1}{Y}\frac{\partial Y}{\partial V_{th}}\sigma V_{th} + \frac{1}{Y}\frac{\partial Y}{\partial \beta}\sigma\beta \tag{10}$$

$$\sigma(\frac{\Delta I_d}{I_d})^2 = (\frac{g_m}{I_d})^2 \cdot \sigma(\Delta V_{th})^2 + \left[1 - \left(\frac{g_m}{2} + G_d\right)\cdot R_{SD}\right]^2 \cdot \sigma(\frac{\Delta\beta}{\beta})^2 + \left(\frac{g_m}{2} + G_d\right)^2 \cdot \sigma(\Delta R_{SD})^2 \tag{11}$$

$$\sigma(\frac{\Delta Y}{Y})^2 = \frac{\beta \cdot V_d \cdot \sigma(\Delta V_{th})^2}{4 \cdot \beta \cdot V_d \cdot n^2 \cdot (kT/q)^2 + Y^2} + \frac{1}{4} \cdot \sigma(\frac{\Delta\beta}{\beta})^2 \tag{12}$$

where $\sigma(\Delta V_{th})$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{SD})$ are the standard deviations of the threshold voltage, current gain parameter and source-drain access resistance, respectively. $g_m = \mathrm{d}I_d/\mathrm{d}V_g$ is the transconductance and $G_d = I_d/V_d$ is the output ohmic conductance. The full model [9–11] could also include the variability of the subthreshold slope SS through the standard deviation of subthreshold slope ideality factor $\sigma(\Delta n)$, but it was overlooked in this work as being negligible. The variability of current gain parameter $\Delta\beta/\beta$ can have an impact in strong inversion ($V_g > V_{th}$), mainly due the variability of effective gate length L_{eff}, effective width, W and/or mobility μ_0. The variability of the threshold voltage ΔV_{th} mainly stems from fluctuations in channel doping level and/or gate oxide interface charges and has a larger influence near and below threshold [7–11].

The drain current standard deviations versus gate voltage curves are shown in Figure 8 (symbols) for GaN MIS-HEMTs for different gate lengths and wafers. The best fit characteristics (dashed line) obtained with the variability model of Eq. (11) are also reported in the same graphs corresponding to each wafer. This model enables to extract a set of three variability parameters such as $\sigma(\Delta V_{th})$, $\sigma(\Delta\beta/\beta)$ and $\sigma(\Delta R_{SD})$. In strong inversion region, Figure 8a shows an increase of standard deviation $\sigma(\Delta I_d/I_d)$ level with gate bias due to the variability impact of source-drain access resistances $\sigma(\Delta R_{SD})$. This increase depends on the gate length and is less pronounced for long channel length (50 µm) as compared to short channel one (0.5 µm, Figure 8a). This phenomenon disappears on wafers #2 (Figure 8b) and #3 (Figure 8c) thanks to the optimized ohmic contact fabrication process. However, the wafers #2 and #3 are more sensitive to the variability of gain factor $\sigma(\Delta\beta/\beta)$ and threshold voltage $\sigma(\Delta V_{th})$.

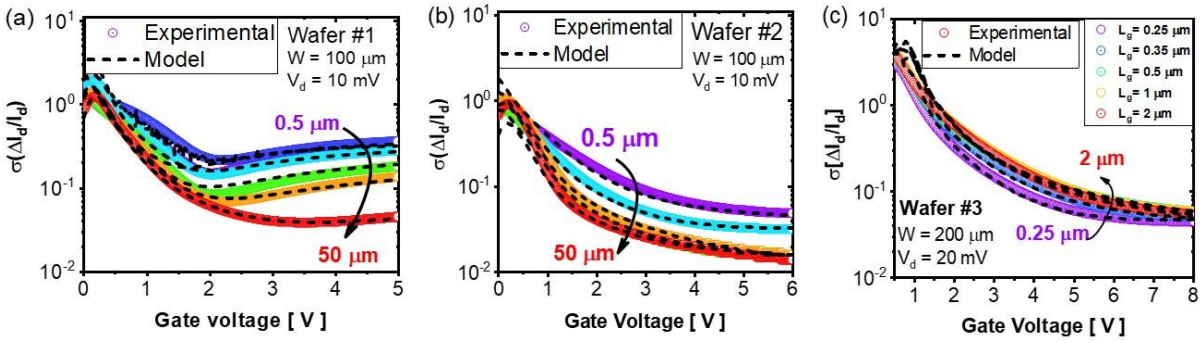

Figure 8. Comparison between experimental data (symbols) and model (dashed line) of the variations of drain current standard deviation $\sigma(\Delta I_d/I_d)$ for different gate lengths versus gate voltage obtained on GaN/Si MIS-HEMT wafers (a) #1, (b) #2 et (c) #3.

The standard deviation of variability dependence with gate length around threshold shows different levels for the various wafers. Compared to wafers #1 and #2, wafer #3 presents a higher level of the standard deviation $\sigma(\Delta I_d/I_d)$ of about a half-decade below the threshold ($V_g < V_{th}$), because $\sigma(\Delta V_{th})$ has a largest impact in subthreshold region, as mentioned previously. Instead, for wafer #2 and #3, $\sigma(\Delta\beta/\beta)$ is predominant in strong inversion and its contribution is even larger for higher gate bias, because the access resistance variability contribution is reduced since the value of their HEMT access resistance is smaller.

In Figure 9 we summarized different variability parameters $\sigma(\Delta V_{th})$, $\sigma(\Delta\beta/\beta)$ et, $\sigma(\Delta R_{SD})$ which were extracted by modelling on wafers #1, #2 and #3. As suggested previously from drain current standard deviation characteristics, a higher variability of threshold voltage $\sigma(\Delta V_{th})$ is obtained on wafer #3 as compared to wafers #2 and #3 (Figure 9a). However, the variability of current gain parameter $\sigma(\Delta\beta/\beta)$ is estimated between 1 and 10 (%) for all wafers (Figure 9b). Compared to the wafer #2 and #3, wafer #1 shows the largest (up to 2 decades) variability of source-drain access resistance $\sigma(\Delta R_{SD})$ in line with its higher mean value and likely due to the degraded ohmic contacts fabrication process (Figure 9c). Note that, for GaN technologies, a larger variability of the threshold voltage $\sigma(\Delta V_{th})$ could originate as for silicon technologies from prevailing role of channel doping variability and/or oxide interface charges fluctuations. This phenomenon is larger for small gate lengths and/or large device widths due to the increased contribution of the gate sidewalls (or gate corners) on the overall device operation.

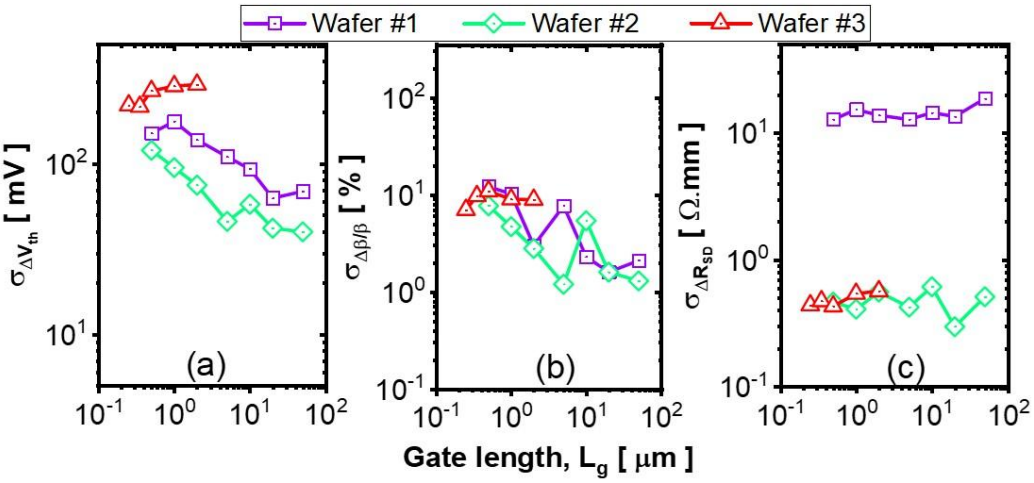

Figure 9. Variation of standard deviations (a) σ(ΔV_{th}), (b) σ(Δβ/β) et (c) σ(ΔR_{SD}) versus gate length for different GaN/Si wafers.

Since $Y(V_g)$ is immune of source-drain access resistance effects, the experimental data of $\sigma(\Delta Y/Y)$ were fitted with the model of Eq. (12) using adjusted parameter $\sigma(\Delta V_{th})$ and $\sigma(\Delta\beta/\beta)$. These values found were then used to fit $\sigma(\Delta I_d/I_d)$ with the additional parameter $\sigma(\Delta R_{SD})$. Figure 10 shows the standard deviation $\sigma(\Delta Y/Y)$ of the Y-function variability extracted on the same data of Figure 2 for different gate lengths along with the modelling results obtained with Eq. (12) (dashed line).

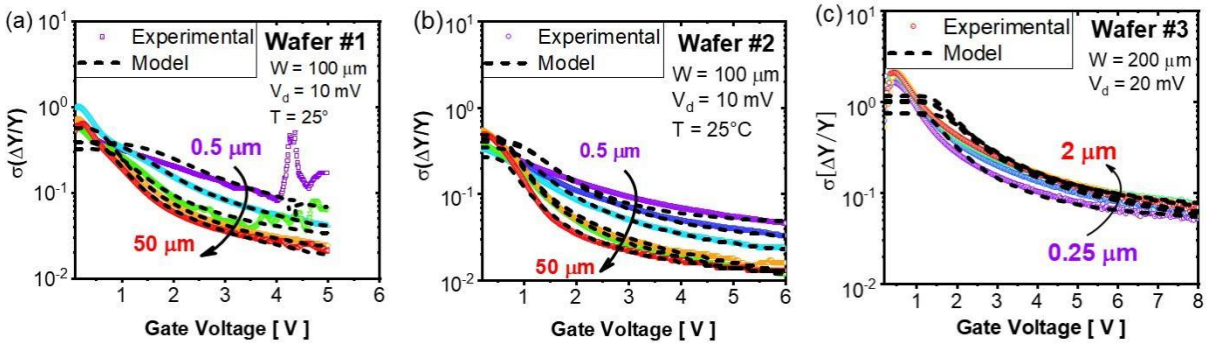

Figure 10. Comparison between experimental data (symbols) and model (dashed line) of the variations of Y-function standard deviation σ(ΔY/Y) for different gate length versus gate voltage obtained on different GaN/Si MIS-HEMT wafers (a) #1, (b) #2 et (c) #3.

Another interesting parameter in variability analysis is the so-called input referred global variability parameter. It gives a best observation between the variability results and can be made by plotting the input referred global variability parameter versus gate bias. This input referred global variability parameter is defined by [9–11]:

$$\sigma_{\Delta V_g} = \frac{\sigma(\Delta I_d/I_d)}{g_m/I_d} \tag{13}$$

Figure 11 shows the input referred global variability parameter $\sigma_{\Delta V_g}$ versus gate bias for different gate lengths and for different wafers #1 (Figure 11a), #2 (Figure 11b), and #3 (Figure 11c). The input referred global variability parameter shows a plateau at low gate bias close to threshold and below, whose value is approximately given by $\sigma_{\Delta V_{th}}$ (such as $\sigma_{\Delta V_{th}} = \min \text{of } \sigma_{\Delta V_g}$ around threshold). In strong inversion, for $V_g > V_{th}$, the $\sigma_{\Delta V_g}$ characteristics increase due to the additional contributions of $\sigma_{\Delta R_{SD}}$ (see Figure 11a) and $\sigma_{\Delta\beta/\beta}$ (Figure 11b and 11c). As can be seen from Figs. 11, these inputs referred global variability data can also be well fitted with the variability model of Eq. (13) using the same set of parameters already employed in Figs. 8 and 10.

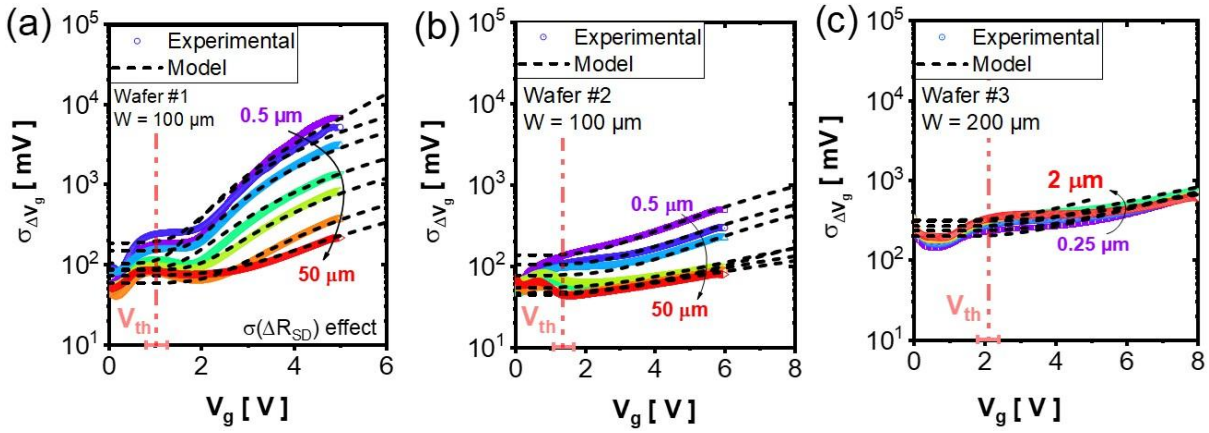

Figure 11. Comparison between experimental data (symbols) and model (dashed line) of the input referred global variability parameter $\sigma_{\Delta V_g}$ for different gate lengths versus gate voltage obtained on GaN/Si MIS-HEMT of wafers (a) #1, (b) #2 et (c) #3.

The standard deviation of V_{th} variability can be advantageously converted into a standard deviation of the oxide interface charge fluctuation $\sigma_{\Delta Q_{ss}}$ (see Eq. 14) in order to estimate their amplitude.

$$\sigma_{\Delta Q_{ss}} = \frac{\sigma_{\Delta V_{th}} \cdot C_{ox}}{q} \left(q/cm^2 \right) \tag{14}$$

Table 2 summarizes all the values obtained for the variability parameters $\sigma_{\Delta V_{th}}$, $\sigma_{\Delta\beta/\beta}$, $\sigma_{\Delta R_{SD}}$ as well as $\sigma_{\Delta Q_{ss}}$ extracted on our GaN/Si MIS-HEMT devices. The $\sigma_{\Delta Q_{ss}}$ values found for such GaN MIS-HEMTs lies in the range 0.6 to $4\times10^{11} q/cm^2$, which is about 2 decades higher than those one can deduce for Silicon technologies with same 100 µm² geometry ($2 \sim 4\times10^{9} q/cm^2$) [7–11]. This is likely due to the lack of maturity of such research-level GaN MIS-HEMT technology and indicates that much improvement could be made after proper process optimization in the future.

Table 2. Extracted variability parameters for this GaN/Si MIS-HEMT technology.

Global Variability Parameters	Wafer #1	Wafer #2	Wafer #3
L_g range [µm]	0.5 to 50	0.5 to 50	0.25 to 2
C_{ox} [$\times10^{-7} F\cdot cm^{-2}$]	2.8	2.6	2.1
$\sigma_{\Delta V_{th}}$ [mV]	[60–150]	[40–120]	[220–300]
$\sigma_{\Delta Q_{ss}}$ [$\times10^{11} q/cm^2$]	[1–3]	[0.6–2]	[3–4]
$\sigma_{\Delta\beta/\beta}$ [%]	[1–12]	[1–10]	[1–10]
$\sigma_{\Delta R_{SD}}$ [$\Omega\cdot mm$]	[12–19]	[0.4–0.7]	[0.4–0.5]

Finally, the contribution of channel resistance variability to the total variability of the GaN MIS-HEMT devices %CH can be evaluated using the variability model of Eq. (11) as [9–11]:

$$\%\mathrm{CH} = \frac{\sigma(\Delta I_d/I_d)^2 \big|_{\sigma(\Delta R_{sd})=0}}{\sigma(\Delta I_d/I_d)^2} \times 100 \tag{15}$$

Figure 12 shows typical variations of the channel contribution %CH (respectively, source-drain access resistance contribution $\%\mathrm{SD} = 1 - \%\mathrm{CH}$) versus gate voltage. As expected, it clearly indicates that wafer #1 suffer more source-drain access resistance variability than wafers #2 and #3.

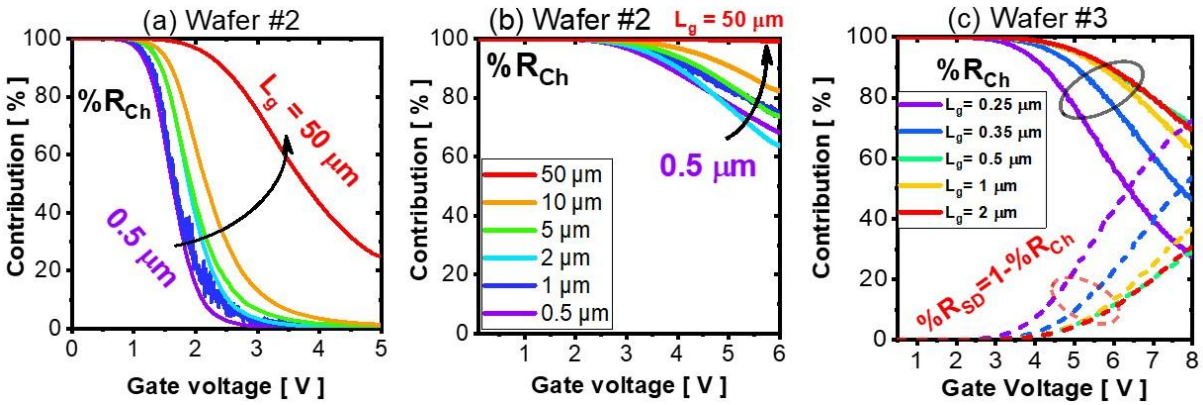

Figure 12. Variations for different gate length versus gate voltage of channel contribution (R_{CH}) in percentage (respectively source-drain access resistances contribution R_{SD}) to the total device global variability for GaN/Si MIS-HEMT wafers (a) #1, (b) #2 et (c) #3.

4. Conclusion

In this work, a detailed study of global variability of the GaN MIS-HEMTs drain current characteristics on 200-mm silicon wafers has been presented here for the first time. The main global variability parameters of GaN MIS-HEMT technology have been extracted using experimental data and the analytical global variability model initially developed for Silicon technology. The global variability analysis is also used on Y-function characteristics showing thus the intrinsic channel variability parameters such as for threshold voltage and gain parameter. The results also show that the variability performances found on different GaN/Si MIS-HEMTs from 200-mm wafers are not as good as those achieved in Silicon CMOS technologies. The key parameters which affect the variability are the oxide interface charge fluctuations, the mobility fluctuations, the gate oxide thickness and/or the gate area variations and access resistance fluctuations in the contact as well as in the 2DEG regions (source and drain sides). This reveals that such research-level GaN/Si MIS-HEMT technology has not reached their full maturity and that much improvement margins are possible after proper GaN technology process optimization.

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Data Availability Statement

The Figure’s data used to support the findings of this study are available from the corresponding author upon request.

Conflict of Interest

There is no conflict of interest for this study.

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