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Article

17 Level Hybrid Diode Clamped Inverter With Reduced Number of Components

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Abstract: Multilevel inverters (MLIs) are gaining more interest recently in medium to high power applications. The main problem with various MLI topologies is that they require a large number of switching devices and DC voltage sources while producing a small number of voltage levels. Which results in bulky inverters with high cost and high output voltage/current total harmonic distortion (THD). This paper introduces a new novel asymmetrical 17-level MLI design using two DC voltage sources and a reduced number of switches. This was achieved by combining a voltage summing and subtracting circuit with a modified diode clamped MLI (DC-MLI), which divides the voltage by two. Thus, generating more voltage levels. nearest level control (NLC) is used to produce the switching signals at a switching frequency of 50Hz. The design is tested and simulated using MATLAB/Simulink, the output voltage THD is kept around 5.7%. The obtained results are compared with other recent 17-level topologies, showing that a good improvement is achieved.

***Keywords*:** multilevel inverter, nearest level control, neutral point clamped, Simulink, switching devices, THD

1. Introduction

The main two types of inverters are pulse width modulation (PWM) inverters and Multilevel Inverters, MLI topologies include flying capacitor (FC), diode clamped and cascaded H-Bridge (CHB) multilevel inverters [1]. Some of the advantages of MLIs are having lower Total Harmonic Distortion, higher output power and no need for output filtering [2,3]. Due to these advantages, MLIs caught the attention of researchers lately and they are used widely in photovoltaic (PV) systems [4], electric vehicles (EVs) [5], and uninterruptable power supplies (UPS) [6–8].

One problem in the various designed MLIs is the large number of switches and DC sources which increases the cost and the size of the inverter [9]. Another problem arises when the number of levels is small; This increases the THD and causes a large *dv*/*dt* stress over the switching devices [10,11].

In [11], a seven level PWM inverter utilizing three series connected capacitors was designed; The three series capacitors divide the input voltage into three equal quantities which can be used to generate the seven voltage levels. One of its advantages is the need for one voltage source and seven switches only. However, the three capacitors need careful balancing to ensure right operation of the inverter, and it generates only seven levels. Paper [12] introduces a modified five level (DC-MLI), the design was achieved by adding two switches to the traditional three level DC-MLI, which provided the ability to utilize the voltage of the source in addition to the DC bus capacitors voltages, the design uses a single source and six unidirectional switches. However, the number of levels is considered to be low. [13] introduced an asymmetrical 17-level inverter using 11 unidirectional switches, which is a good improvement. But it requires 3 DC sources that increase the size and the cost of the inverter.

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In this paper the proposed design reduces the number of components, introduces a comparable low-cost low complexity inverter with high number of levels and an acceptable voltage THD.

2. Proposed Design

The general idea of the proposed design is to combine two circuits, one of which adds and subtracts the two input voltages, whereas the other divide the DC voltage by two, this way more levels can be generated from a given number of sources [14].

2.1 *Circuit Description*

The circuit design is shown in Figure 1, it consists of 12 switches SW1–12, two DC sources V_A and V_B, two diodes and two capacitors. The best ratio for the DC sources, V_B:V_A was found to be 1:5 by using a designed code.

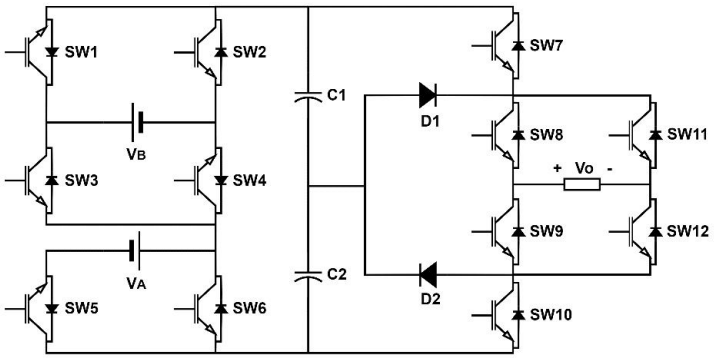


Figure 1. Proposed Topology.

Assume we have n number of voltage levels L, L_0, L_1, L_2…, L_n. The algorithm will calculate the distance D_n between adjacent levels for every ratio of V_B:V_A as follows:

$$\begin{aligned} D_1 &= L_1 - L_0 \\ D_2 &= L_2 - L_1 \\ D_n &= L_n - L_{n-1} \end{aligned} \tag{1}$$

To produce voltage levels that are equally spaced from each other as much as possible (to reduce the *dv*/*dt* stress and the THD.), the difference between the distances should ideally equal zero, but since the levels are asymmetrical this is not possible; Therefore, the algorithm iterates through equation (2), and it outputs the best ratio.

$$D_2 - D_1 = D_3 - D_2 \cdots D_n - D_{n-1} = 0 \tag{2}$$

The design can be divided into two sections as shown in Figure 2.

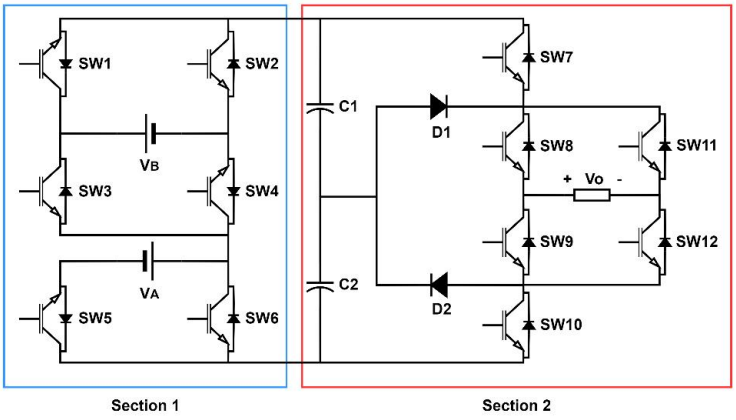


Figure 2. The Two Main Sections of the System.

The first section consists of SW1–6, and it is a modified version of a design proposed by [15], this circuit can generate four voltage levels, namely: V_A, V_B, V_A+V_B, V_A-V_B. The second section is a modified diode clamped inverter introduced in [12], which can divide the voltage by a factor of two, so the output of this section will be the voltage levels from section one divided by two: $V_A/2$, $V_B/2$, $(V_A+V_B)/2$, $(V_A-V_B)/2$. Switches SW11 and SW12 can provide a path to switch the output between section one and the diode clamped circuit. Also, switches SW8, SW9, SW11 and SW12 act like an H-Bridge and provide inversion for the output voltage.

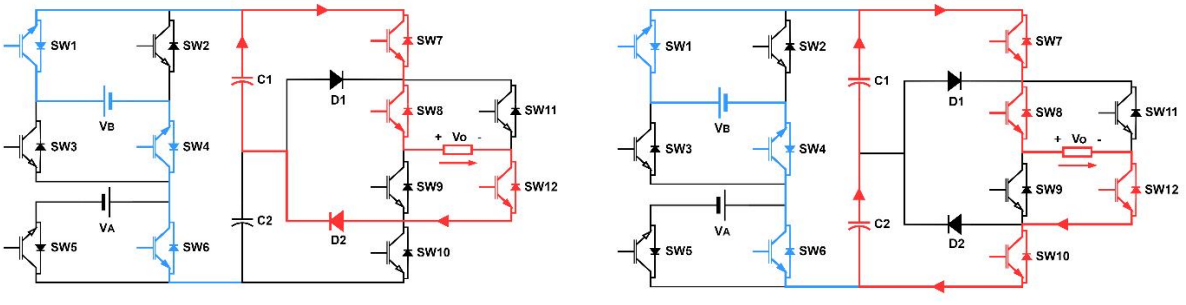
2.2 *Modes of Operation*

The states of the switches are shown in Table 1, where (0) indicates that the switch is off, (1) indicates it is on and an (×) means the state can be on or off as it does not affect the output voltage. Modes 1–8 are the positive half cycle, mode nine is the zero level and modes 10–17 are the negative half cycle.

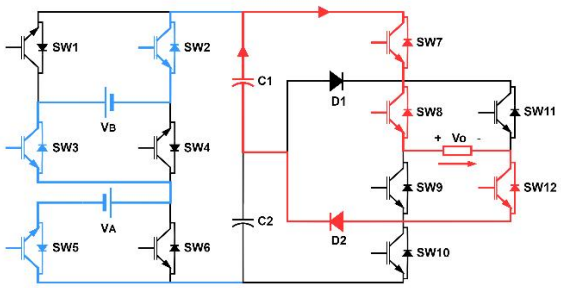
Table 1. Switching Sequence for The Proposed Design

		Switches State											
Modes	Vo	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
1	$V_B/2$	1	0	0	1	0	1	1	1	0	0	0	1
2	V_B	1	0	0	1	0	1	1	1	0	1	0	1
3	$(V_A-V_B)/2$	0	1	1	0	1	0	1	1	0	0	0	1
4	$V_A/2$	0	1	0	1	1	0	1	1	0	0	0	1
5	$(V_A+V_B)/2$	1	0	0	1	1	0	1	1	0	0	0	1
6	V_A-V_B	0	1	1	0	1	0	1	1	0	1	0	1
7	V_A	0	1	0	1	1	0	1	1	0	1	0	1
8	V_A+V_B	1	0	0	1	1	0	1	1	0	1	0	1
9	0	×	×	×	×	×	×	×	0	1	0	0	1
10	$-V_B/2$	1	0	0	1	0	1	0	0	1	1	1	0
11	$-V_B$	1	0	0	1	0	1	1	0	1	1	1	0
12	$-(V_A-V_B)/2$	0	1	1	0	1	0	0	0	1	1	1	0
13	$-V_A/2$	0	1	0	1	1	0	0	0	1	1	1	0
14	$-(V_A-V_B)/2$	1	0	0	1	1	0	0	0	1	1	1	0
15	$-(V_A-V_B)$	0	1	1	0	1	0	1	0	1	1	1	0
16	$-V_A$	0	1	0	1	1	0	1	0	1	1	1	0
17	$-(V_A+V_B)$	1	0	0	1	1	0	1	0	1	1	1	0

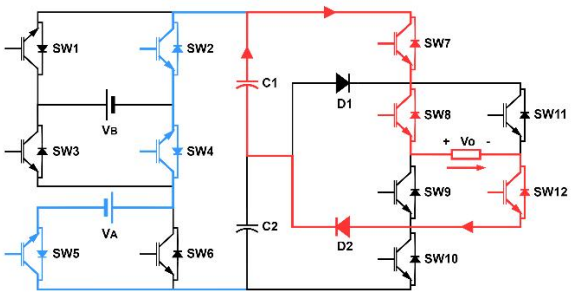
Figure 3 shows all the different configurations that produce the desired 17 voltage levels. The blue lines in section one represent the connections between the two voltage sources, whose output is the input to the DC bus capacitors in section two. In section two the red lines show the current path from the DC bus capacitors to the load.



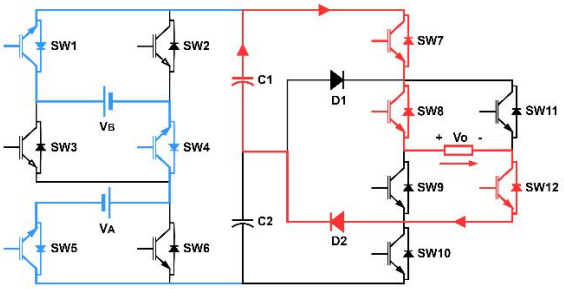
(a) (b)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

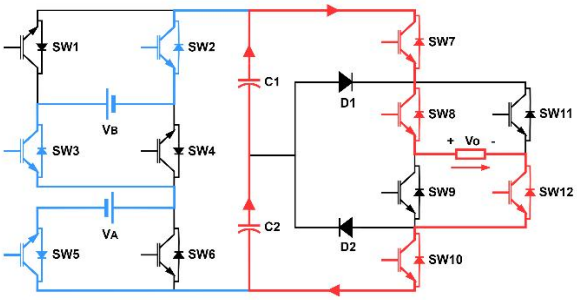
(c)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

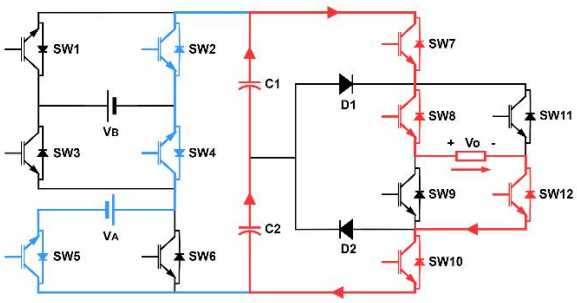
(d)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

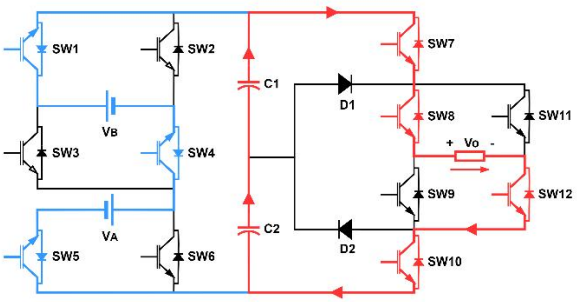
(e)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

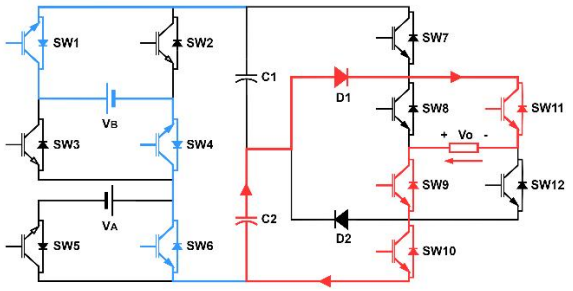
(f)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

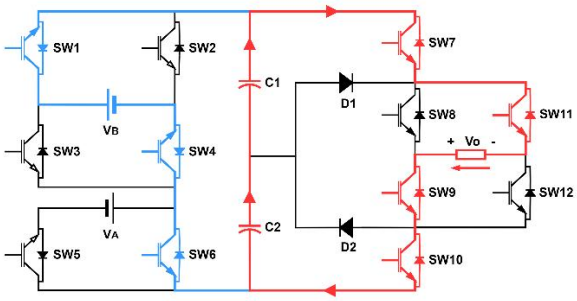
(g)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

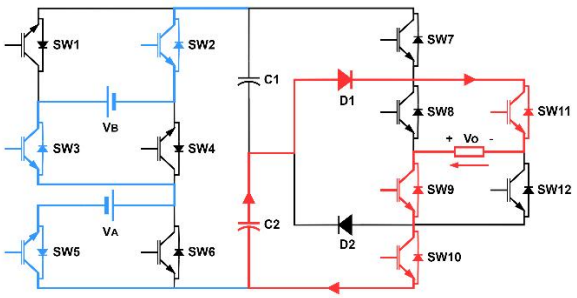
(h)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

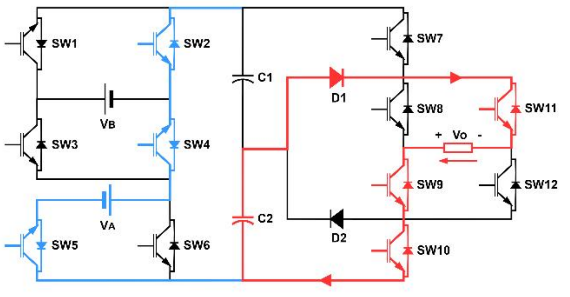
(i)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

(j)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

(k)


SW1
SW2
VB
SW3
SW4
VA
SW5
SW6
C1
C2
D1
D2
SW7
SW8
SW9
SW10
SW11
SW12
+ Vo -

(l)

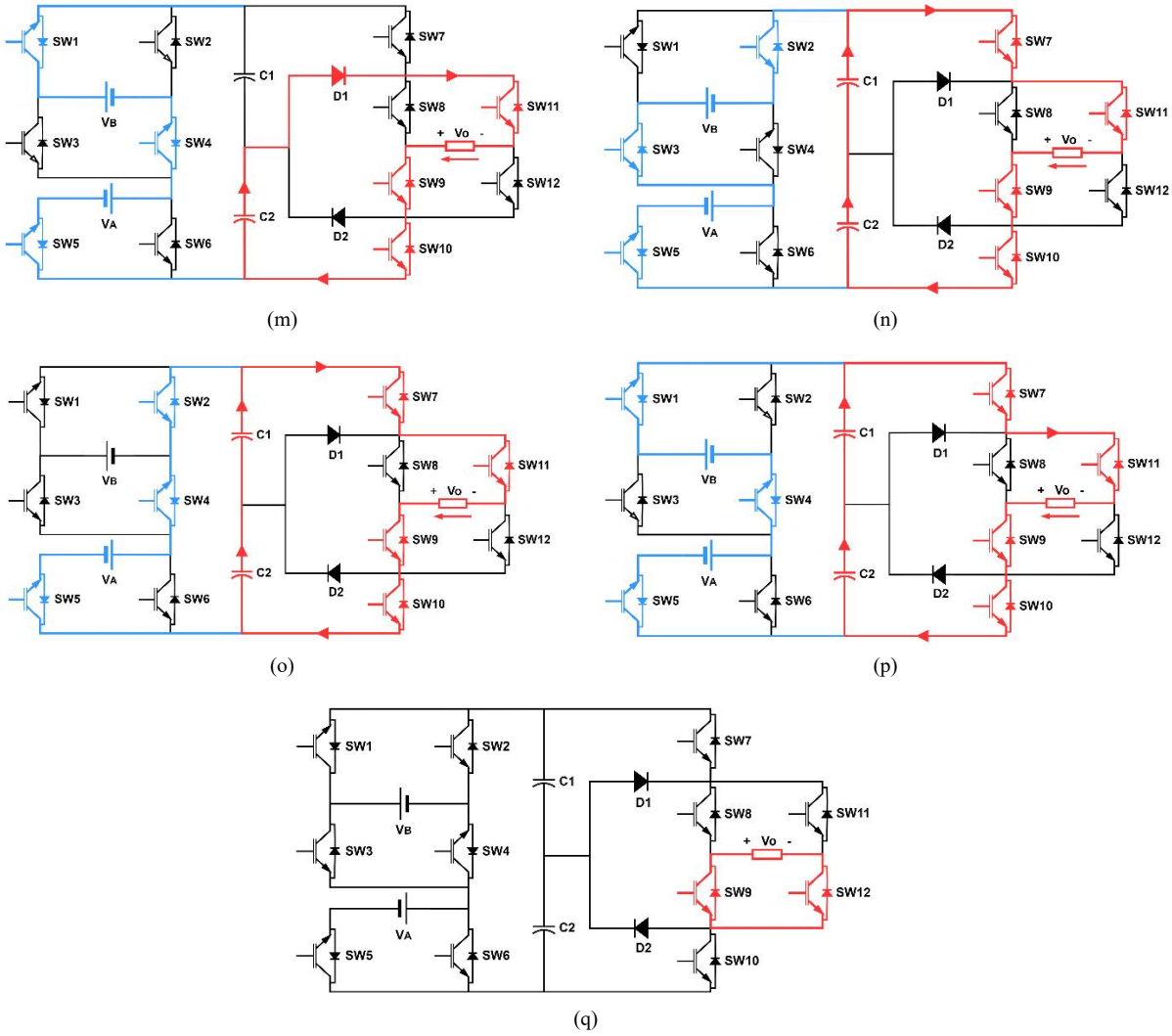


Figure 3. Modes of Operation. (a) VB/2, (b) VB, (c) (VA−VB)/2, (d) VA/2, (e) (VA+VB)/2, (f) VA−VB, (g) VA, (h) VA+VB, (i) −VB/2, (j) −VB, (k) −(VA−VB)/2, (l) −VA/2, (m) −(VA+VB)/2, (n) −(VA−VB), (o) −VA, (p) −(VA+VB), (q) Zero

2.3 *Control Method*

Nearest Level Control (NLC) is a fundamental frequency switching technique used to control the inverter at a switching frequency of 50Hz; Since the voltage levels are asymmetrical using this method simplifies the implementation, because the generated voltage levels can be outputted directly [16,17]. The output voltage at a given moment is determined by checking what is the nearest voltage level at that moment relative to a reference waveform [18,19].

Figure 4 shows the stepped waveform and the corresponding voltage levels for a 50Hz sinewave reference.

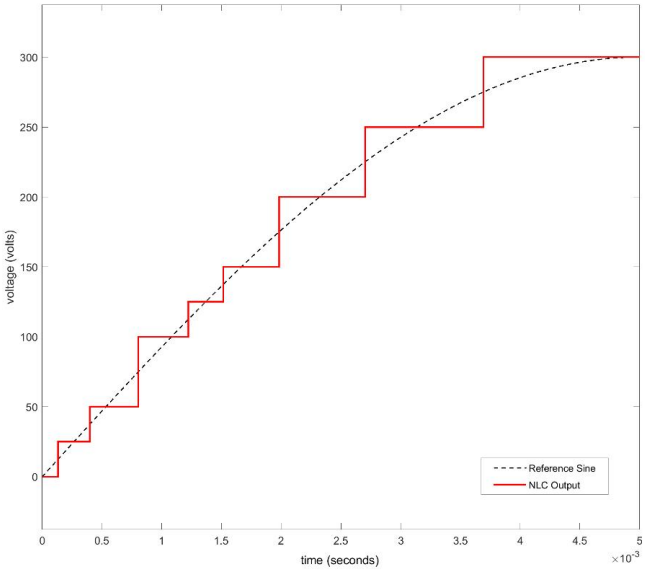
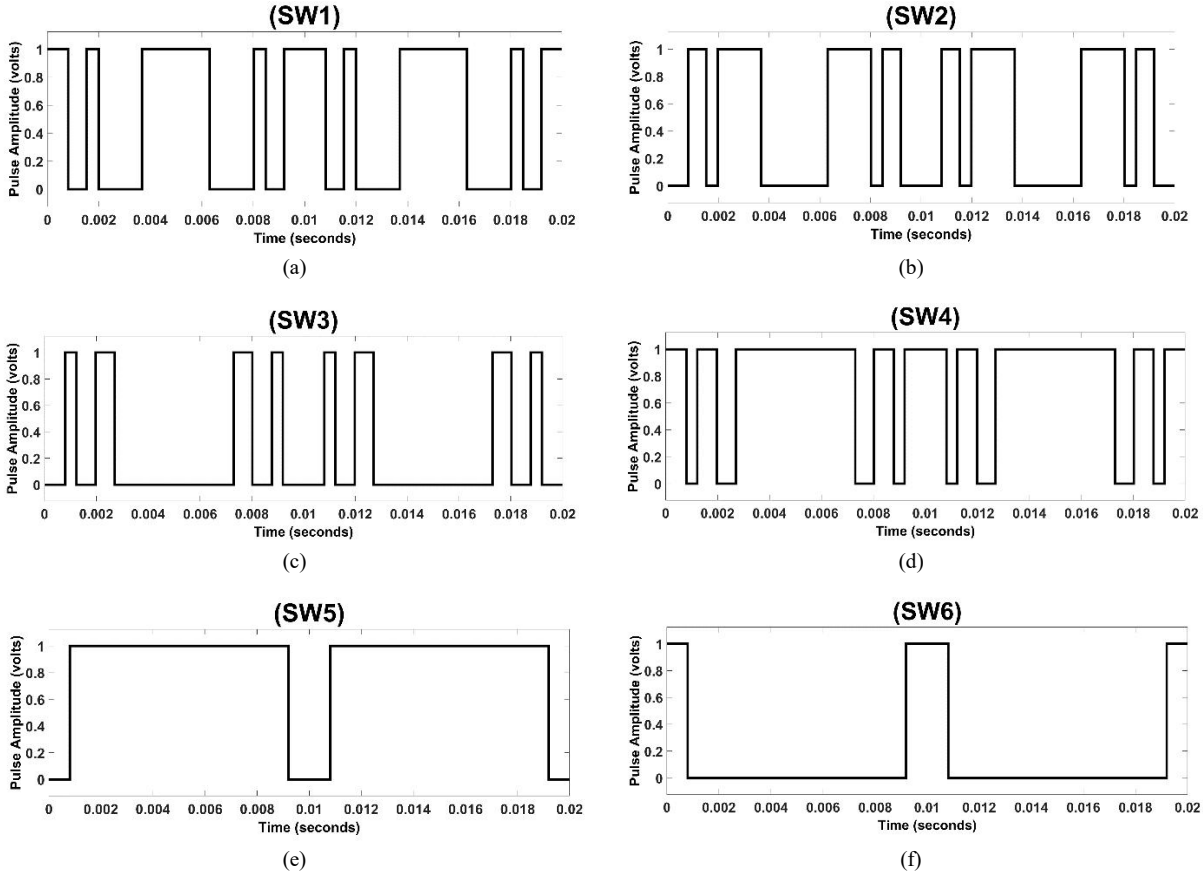


Figure 4. Nearest Level Control

3. Results and Discussion

MATLAB/Simulink software was used to simulate the proposed design at a fundamental frequency of 50Hz, values for the DC sources are V_A = 250 volts and V_B = 250 volts and $C_1 = C_2$ = 4700 µF. The switching pulses were generated using NLC. Figure 5 shows the control signals. Figure 6 shows the SIMULINK Model.



(a) (b) (c) (d) (e) (f)

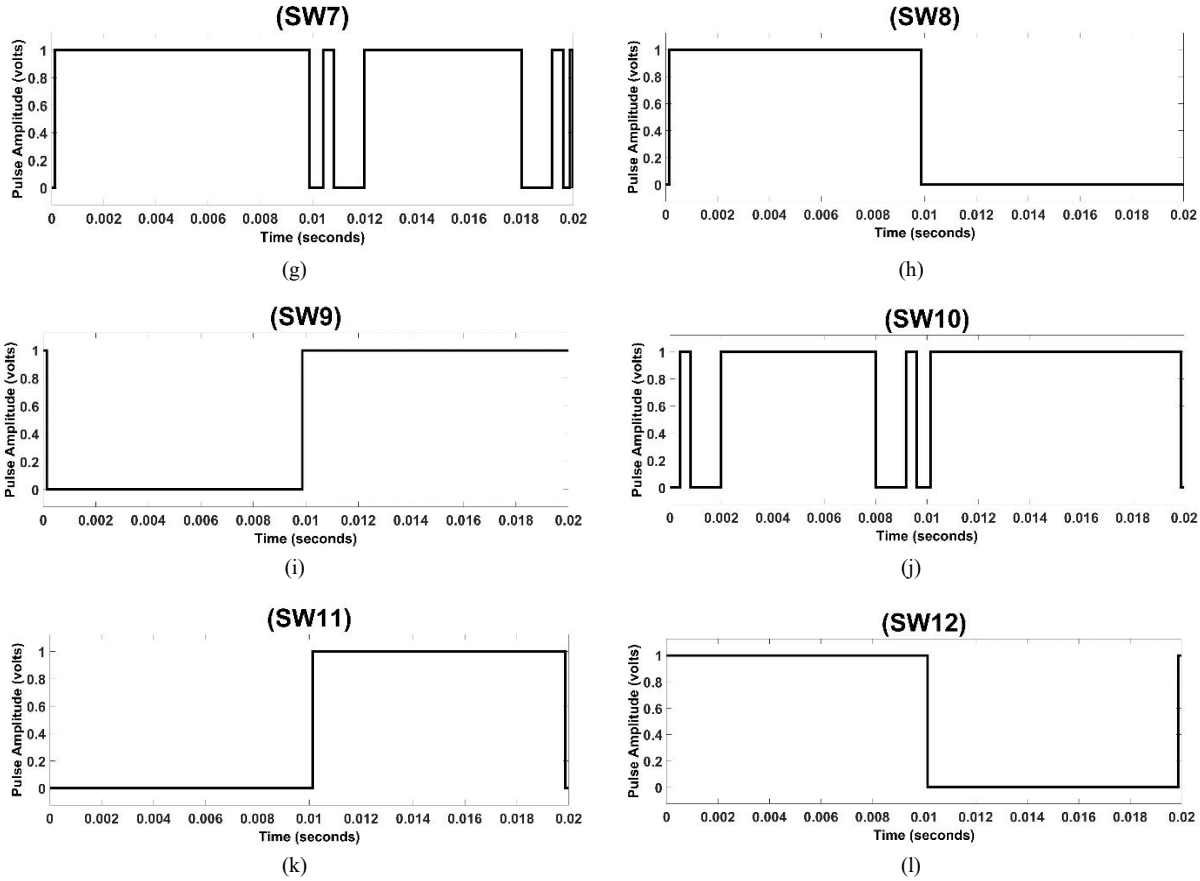


Figure 5. Control Signals

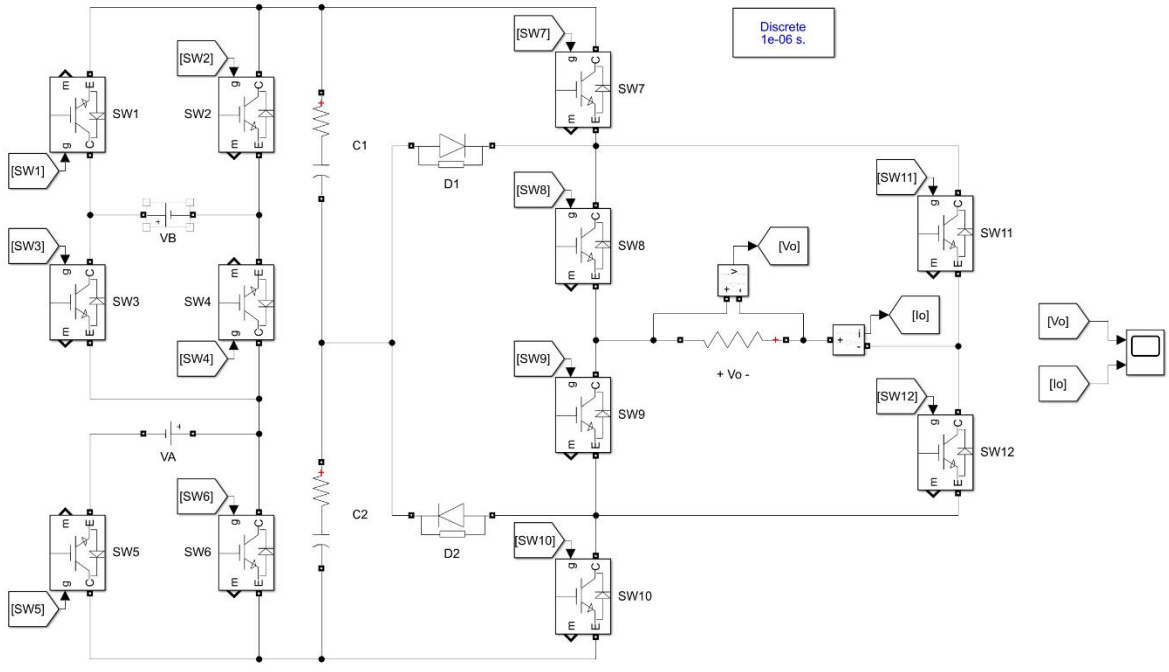
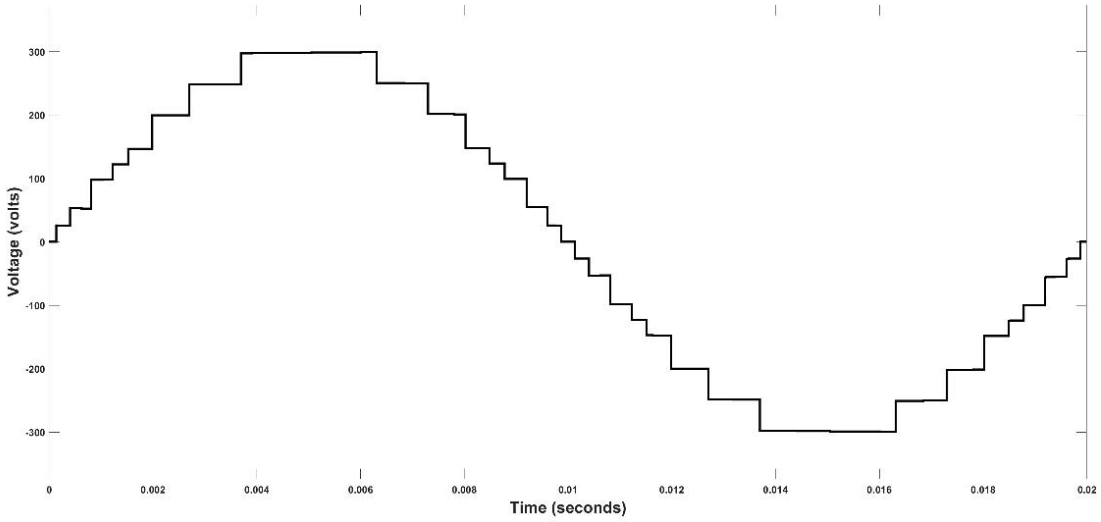
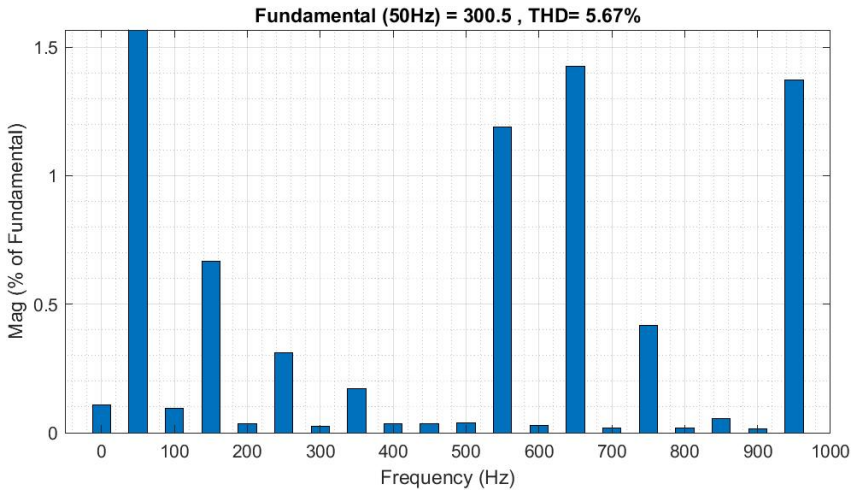


Figure 6. Simulink Model

The design was evaluated for various loads, Figure 7a shows the output voltage for a 10Ω resistive load, and it matches the expected results. The voltage THD is 5.67% as shown in Figure 7b.



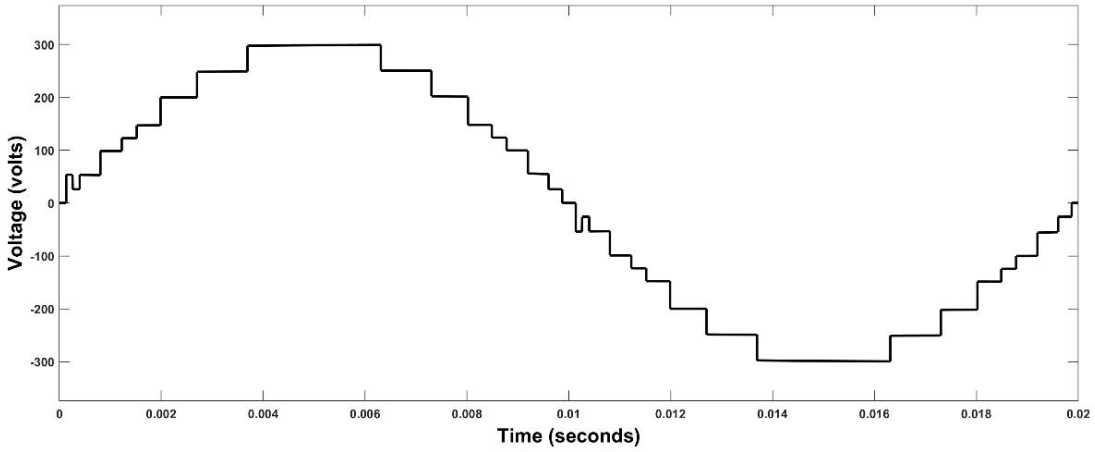
(a)



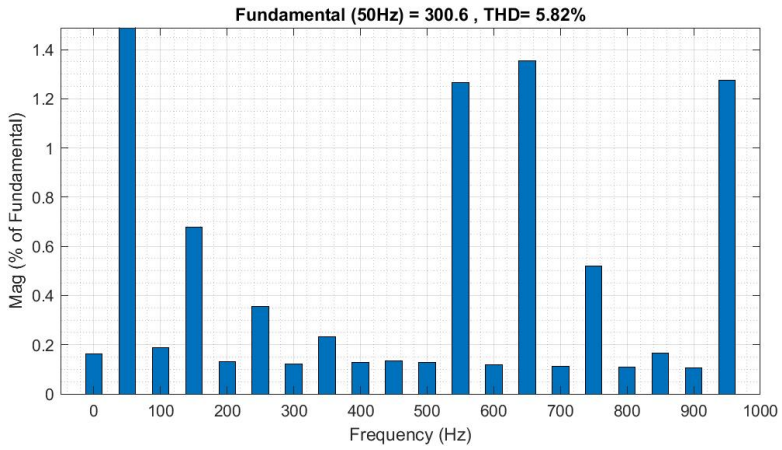
(b)

Figure 7. 10Ω Resistive Load. (a) Output Voltage (b) Voltage THD

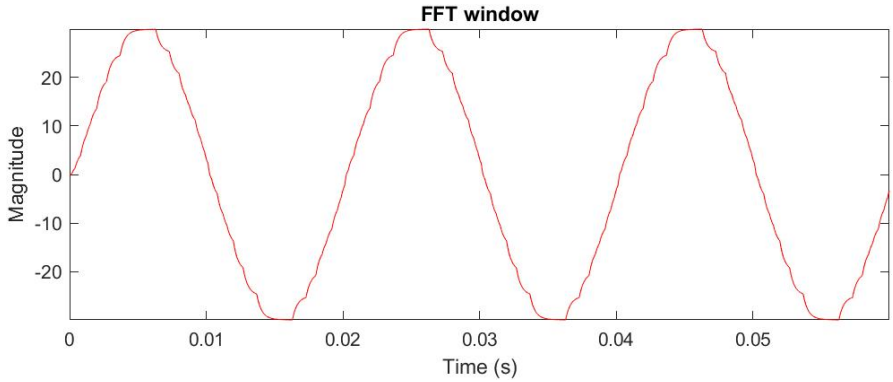
An inductive load of 3.5mH + 10Ω was applied, giving a voltage THD of 5.82% and a current THD of 2.04% as shown in Figure 8a–d. It can be noticed that the voltage THD increased slightly due to distortion added by the inductive load.



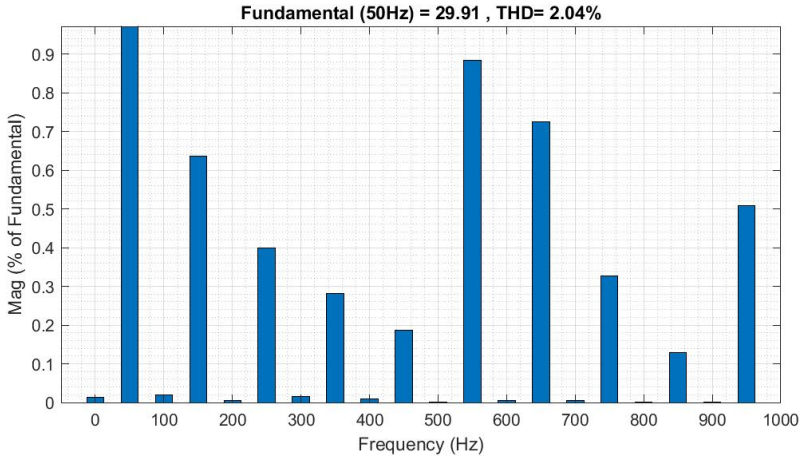
(a)



(b)



(c)



(d)

Figure 8. 3.5mH + 10Ω Inductive Load. (a) Output Voltage (b) Voltage THD (c) Output Current (d) Current THD.

For large inductances (larger than 10mH), the distortion increases as shown in Figure 9 where a 40mh + 20Ω load was applied. The cause of this problem is the lack of a proper path for reverse inductor current at times when voltage is divided by two (i.e., Modes 1, 3, 4, 5, 10, 12, 13, 14), which causes these levels to be bypassed and the output behaves like section 1.

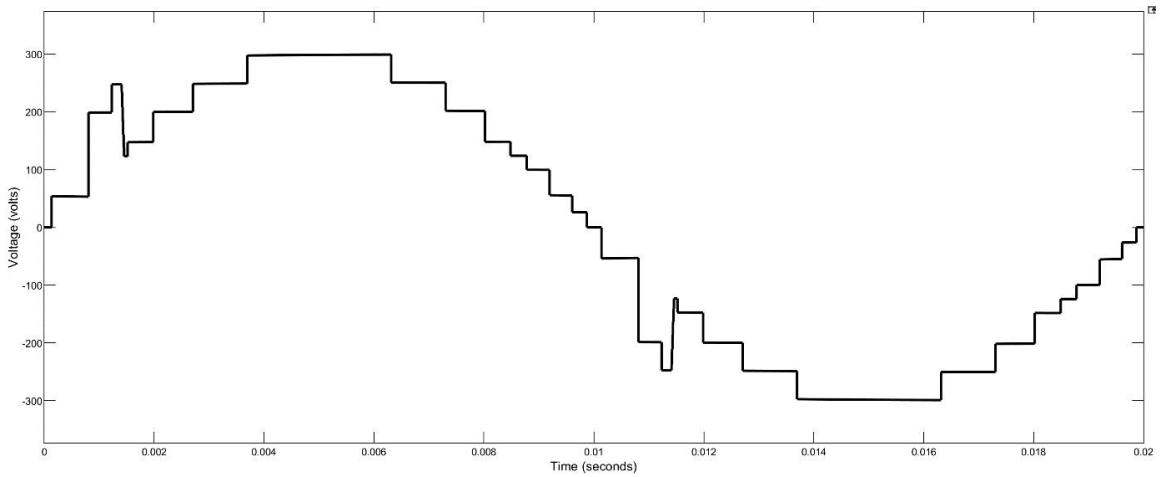


Figure 9. Output Voltage for a 40mH + 20Ω Load.

This can be solved by replacing D1 and D2 with two switches, SW13 and SW14 respectively as shown in Figure 10, thus providing a controlled reverse current path if an inductive load with large inductance is applied. Control signals for SW13 and SW14 are shown in Figure 11 below.

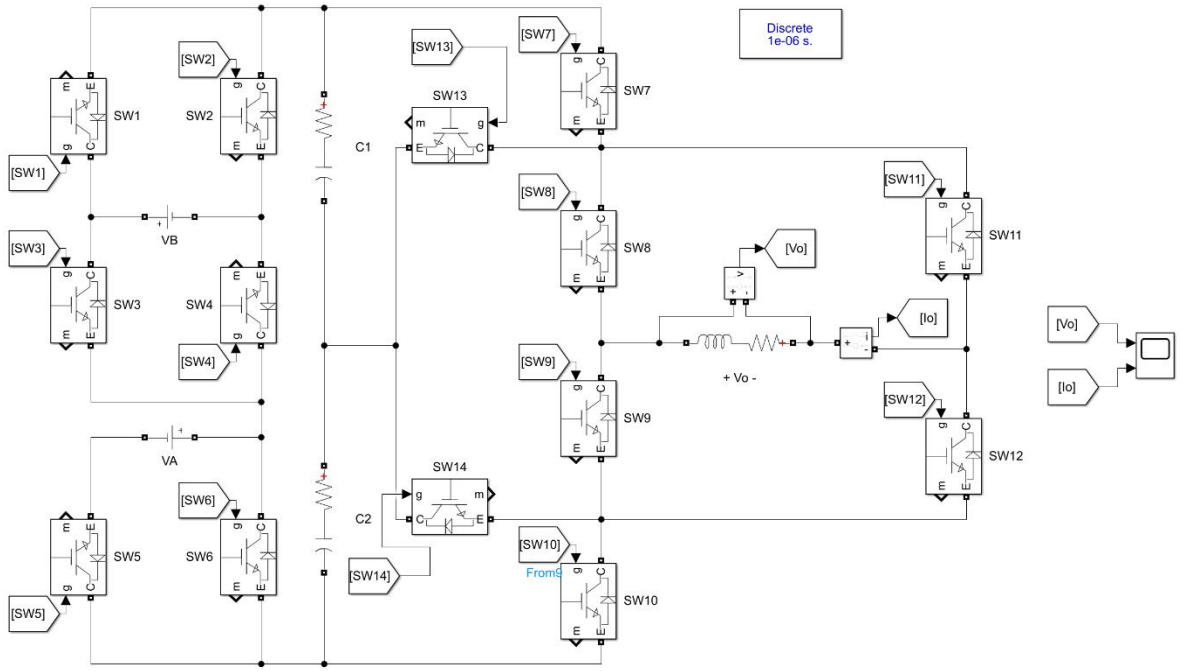


Figure 10. Modified Circuit.

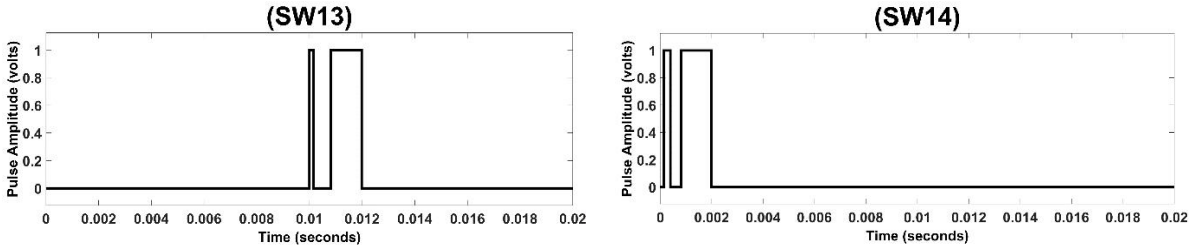
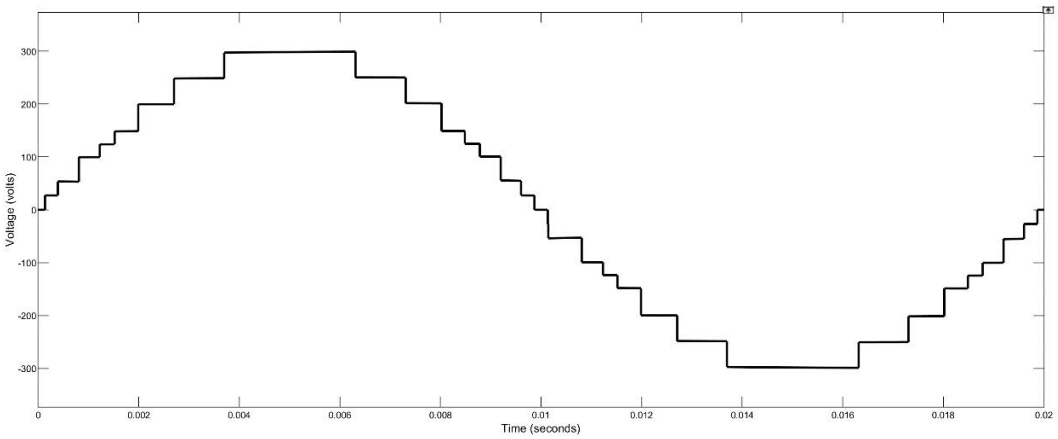
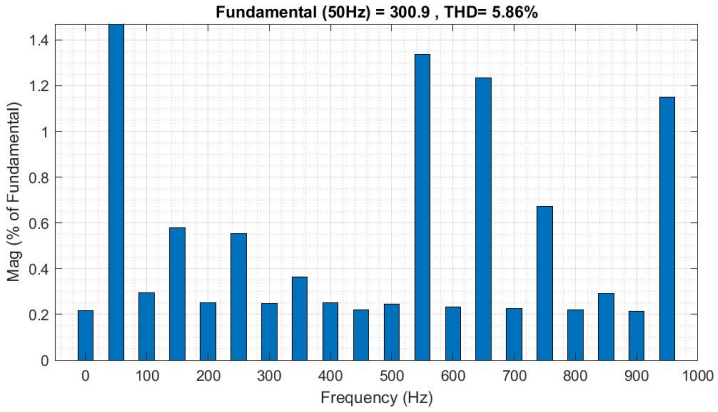


Figure 11. Control Signals for Switches SW13 and SW14.

Figure 12a shows output voltage of the modified circuit for the same 40mh + 20Ω load, it exhibits a voltage THD of 5.86% and a current THD of 0.68% as shown in Figure 13b.

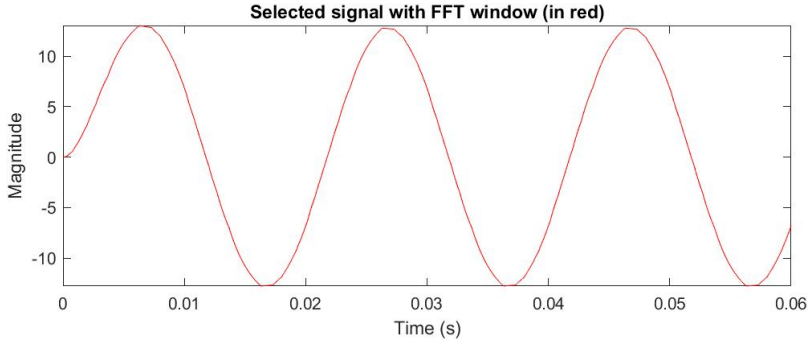


(a)

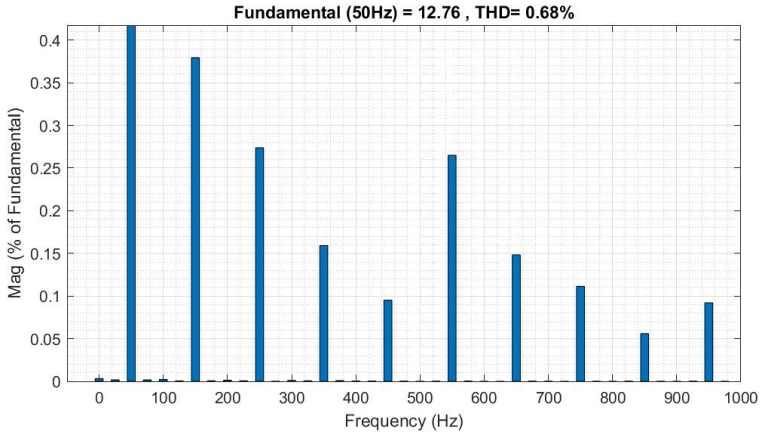


(b)

Figure 12. Modified Circuit Output for 40mH + 20Ω Inductive Load. (a) Output Voltage (b) Voltage THD.



(a)



(b)

Figure 13. Modified Circuit Output for 40mH + 20Ω Inductive Load. (a) Output Current (b) Current THD.

The modified circuit has been tested under a sudden input change as shown in Figure 14, where VA dropped from 250 volts to 210 volts, and VB dropped from 50 volts to 40 volts.

Figure 15 shows a sudden load change condition, where the load changed from 25mh + 7Ω to 40mh + 15Ω.

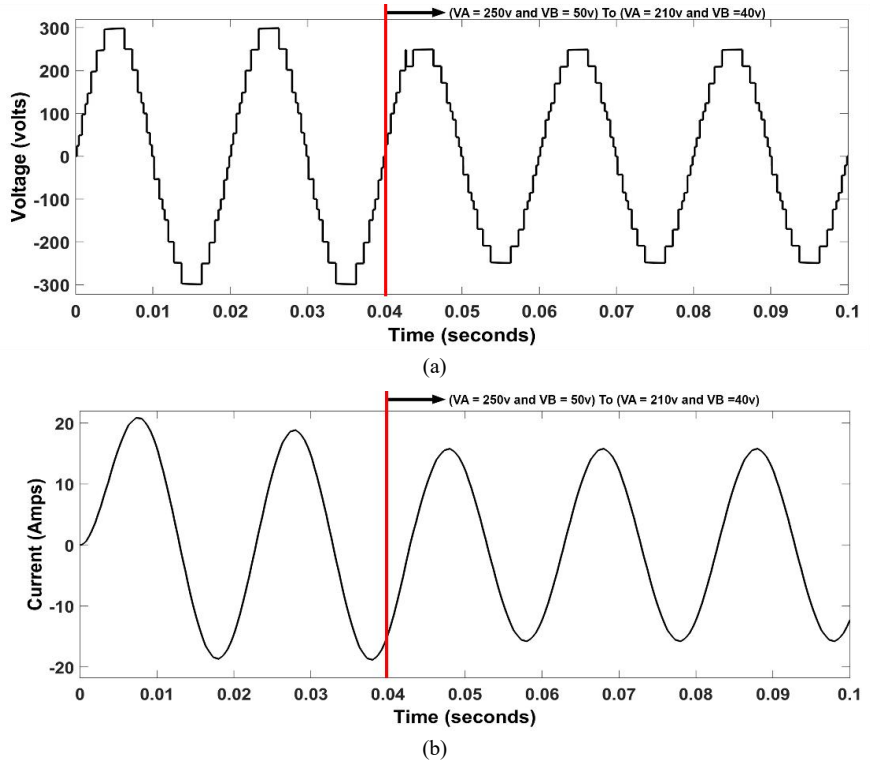


Figure 14. Sudden Input change. (a) Output Voltage (b) Output Current

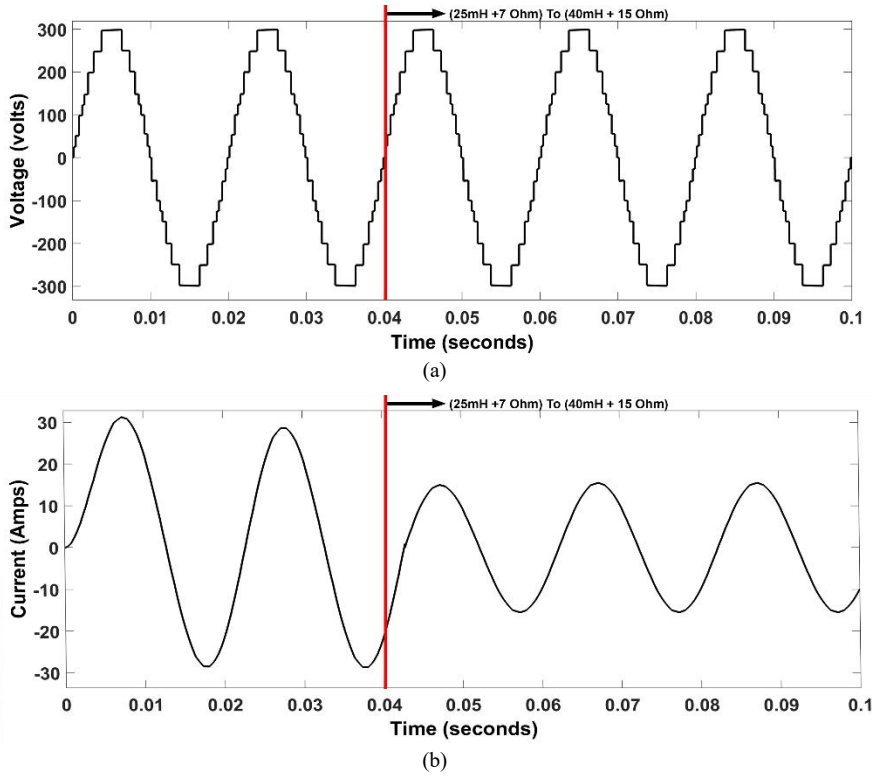


Figure 15. Sudden Load change. (a) Output Voltage (b) Output Current

Two main power loss mechanisms affect switching devices, conduction losses and switching losses; Switching losses are prominent in topologies with high switching frequency, while conduction losses are more

dominant in low switching frequency designs. Since NLC is a low switching frequency technique, switching losses can be neglected.

Conduction losses are caused by the on-resistance of the switch R_S and the anti-parallel diode R_D. The conduction losses of the switch P_{CS} and of the diode P_{CD} can be calculated as follows [16]:

$$P_{CD} = V_S i(t) + \left[R_S i^{\beta}(t)\right] i(t) \tag{3}$$

$$P_{CD} = V_D i(t) + R_D i^2(t) \tag{4}$$

Where V_S is the switch voltage, V_D is the diode voltage and β is a data-sheet constant. The average conduction power loss during a period of time P_C, can be calculated using equation (5) as follows:

$$P_C = \frac{1}{\pi}\int_0^{\pi}\left[N_S(t)P_{CS}(t) + N_D(t)P_{CD}(t)\right]dt \tag{5}$$

Where N_S is the number of switches and N_D is the number of diodes conducing at the time instant t.

The efficiency of the inverter η_{inv} can be found using equation (6):

$$\eta_{inv} = \frac{P_{AC}}{P_{DC}} \tag{6}$$

Where P_{AC} is the output AC power, and P_{DC} is the input DC power. The efficiency in the resistive load case is 92.11%.

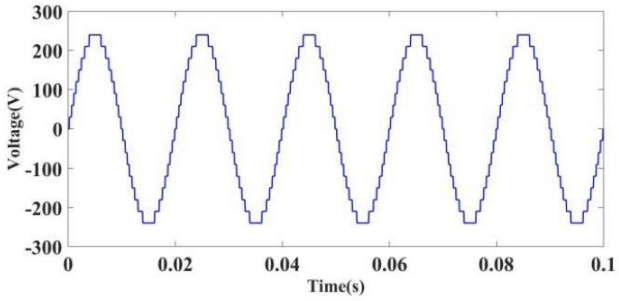
Different 17-level inverters are compared in terms of the number of components in Table 2.

Table 2. Comparison of Various 17-Level Topologies

Feature	[13]	[20]	[21]	Proposed (modified)	Proposed
Switching Devices	11	16	20	14	12
DC Sources	3	4	1	2	2
Capacitors	0	4	4	2	2
Diodes	0	0	2	0	2

Figure 16a shows the output voltage of the design introduced in [13] that uses 11 switches, which is the lowest number of switches in this comparison, but it needs 3 independent voltage sources to operate, this puts it at a disadvantage especially in terms of size. In [20] a CHB-MLI design is introduced, with a total switch count of 16, and four voltage sources and four DC bus capacitors. In one hand, the levels are symmetrical, and the output voltage shown in Figure 16b has a THD of 4.12%, on the other hand, the number of sources, switches and capacitors increases the size and the cost of the inverter dramatically. [21] presented a design utilizing only one voltage source. However, 20 switches are required, in addition to 4 capacitors and two diodes. The output voltage is shown in Figure 16c. Even though one source is needed, the number of switches is the highest among all the compared topologies, and it contributes to a noticeable increase in the cost.

It can be noticed that the proposed designs achieve a balance between the number of switches, DC sources and capacitors. Thus, making it a good candidate for many use cases, without being very bulky or very expensive.



(a)

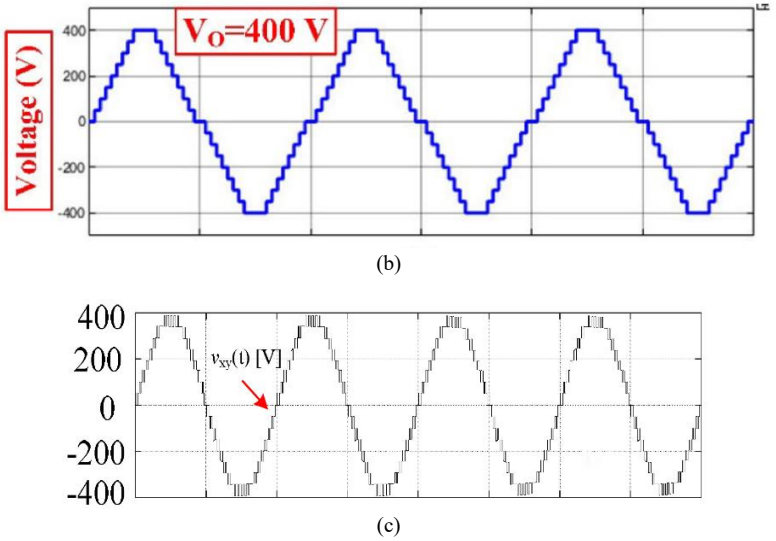


Figure 16. Output voltage of (a) reference [13]. (b) reference [20]. (c) reference [21].

4. Conclusion

In this paper a novel promising multilevel inverter was introduced. The number of components and DC supplies was reduced while keeping a high number of output voltage steps and reasonable THD, the main approach to do that was by combining a DC voltage summing and subtracting circuit with a circuit that divides the DC voltage by two.

An algorithm was written to design an iteration method that gives the best ratio between the two input DC supplies.

Two circuits were designed, both generating 17-levels from two DC sources and two DC bus capacitors; The first one is suitable for resistive loads or low inductance loads (below 10mH), it employs only 12 switching devices. The second circuit (the all-loads circuit) solves a problem related to loads with large inductance by adding two more switches with a total switch count of 14. Both circuits showed good current THD without any filtering or modulation.

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Conflict of Interest

There is no conflict of interest for this study.

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