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Research Article

Improving the ON/OFF Current Ratio and Ambipolarity of Doping-Less Tunneling Carbon-Nanotube FET Using Drain Engineering Technique

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Abstract: This paper presents a novel structure utilizing a doping-less (DL) tunneling carbon nanotube field-effect transistor (T-CNTFET) with dual drain work functionality aimed at enhancing the ON/OFF current ratio. The proposed design features a zigzag carbon nanotube (CNT) of type (13, 0) with a diameter of 1 nm. It employs HfO_2 as the gate oxide, which is 2 nm thick and has a dielectric constant of 16. The CNT serves as an intrinsic semiconductor for the source and drain regions, which are composed of metals with appropriate work functions. By selecting appropriate metals for the source and drain regions, the necessity for doping as a fabrication step is avoided, simplifying construction and reducing costs for the nanoscale device. This design includes two drain electrodes, each measuring 15 nm in length and having different work functions (DWFs). The work function of the drain positioned closest to the channel (DWFAC) is set at 3.9 eV, which is 0.5 eV lower than that of the CNT, while the other drain section has a work function of 3.4 eV, 1 eV lower than the CNT. The electrical properties of the device were examined through quantum numerical simulations using the non-equilibrium Green's function (NEGF) method. The results indicate that the proposed structure significantly decreases the OFF-state current and improves the ON/OFF current ratio. Additionally, the leakage current is substantially lowered, resulting in favorable changes to the device's ambipolarity, along with a reduction in hot carrier effects and subthreshold swing (SS).

***Keywords*:** doping-less T-CNTFET, ON/OFF current ratio, ambipolarity, band-to-band tunneling

1. Introduction

As semiconductor devices continue to shrink into the nanoscale, downsizing silicon transistors has become increasingly challenging. For instance, the Boltzmann equation restricts the subthreshold swing of transistors to approximately 60 mV/dec at room temperature [1, 2, 3]. Inherent limitations such as power consumption, the speed of transitioning from ON to OFF states, and the need for operation at lower supply voltages necessitate the development of new devices. Additionally, MOSFETs are no longer sufficient to meet the standards set by the International Technology Roadmap for Semiconductors (ITRS) [4, 5, 6, 7].

To meet the ITRS requirements, it is essential to adopt new technologies, including the use of carbon-based substances like graphene and carbon nanotubes (CNTs) as channels in transistors [8, 9, 10, 11]. CNTs are especially advantageous for nanotechnology in transistor development owing to their one-dimensional (1D) structure, adjustable band gap, excellent

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electrical conductivity, quasi-ballistic transport characteristics, and elevated Fermi velocity. These structures are composed of single atom thick, cylindrical carbon molecules that create a tube with walls made entirely of carbon atoms.

The distinctive mechanical, chemical, optical, and electrical characteristics of CNTs render them exceptionally valuable for numerous applications including microelectronics, microwave absorption, chemical sensing, electromagnetic interference shielding (EMI), biosensing, and aerospace technologies [12, 13, 14, 15]. Single-walled carbon nanotubes (SWCNTs) are a highly promising option for channels in field-effect transistors (FETs) because of their one-dimensional structure and exceptional structural quality. Carbon nanotube FETs (CNTFETs) demonstrate superior performance compared to conventional silicon transistors, as their 1D band structure minimizes scattering effects [16, 17, 18, 19]. To address the limitations of conventional devices and develop integrated circuits with lower energy consumption, various innovations, such as tunneling carbon nanotube FETs (T-CNTFETs), have emerged.

These devices have garnered significant attention for their low OFF-state current and high subthreshold slope compared to MOSFETs [20, 21, 22, 23]. Additionally, they exhibit a high ON/OFF current ratio, which is a critical advantage. However, T-CNTFETs also face challenges, including low ON-state current, direct source-to-drain tunneling, and ambipolarity [24, 25, 26, 27]. Furthermore, T-CNTFETs face several challenges in the manufacturing process, including the high costs related to ion implantation and the considerable thermal budget required for the high-temperature thermal annealing process. Additionally, the heavy doping levels required for T-CNTFETs make them vulnerable to random dopant fluctuations (RDF), which can adversely affect device performance [28, 29, 30, 31].

One major challenge in miniaturizing transistors is the creation of diode junctions between the source and drain and the channel regions. This issue can potentially be addressed by utilizing a dopoing-less (DL) transistor structure [32, 33, 34]. In doping-less structures, one significant advantage is the elimination of the doping importation step during manufacturing. This contrasts with conventional T-CNTFET structures, where the development of the drain and source metal requires the application of voltage, adding complexity to the manufacturing process [35, 36, 37]. The challenge of incorporating doping into the drain and source regions is notably greater than that of applying a metal coating. As a result, DL structure offers a more streamlined manufacturing process compared to traditional designs, making it a superior option in terms of efficiency and simplicity [38, 39, 40]. In DL transistors, the semiconductor CNT remains intrinsic throughout, with the source and drain regions selected based on metals with appropriate work functions. This design eliminates the need for doping by inducing the source and drain regions through careful work function selection [41, 42, 43, 44, 45].

DL structures are particularly appealing because they help reduce short channel effects (SCEs) and streamline the manufacturing process compared to conventional transistors. The DL technique effectively mitigates the complications associated with abrupt junctions, enhancing fabrication efficiency, scaling capabilities, and overall reliability. Additionally, DL transistors improve ambipolar behavior and reduce high leakage current, which are two significant challenges faced by T-CNTFETs [46, 47, 48, 49, 50, 51]. In recent years, a number of experimental and theoretical studies have been conducted to enhance the performance of T-CNTFETs regarding scaling capabilities and overall figure of merits. Notable advancements include the implementation of hetero-dielectric dual material gate doping-less TFETs [35, 36, 37], the development of junction-less work function engineered gates [38], and the adoption of gate-all-around (GAA) structures [39]. Additionally, techniques combining high-k and low-k gate dielectrics [40], gate-drain overlap [52], and gate-drain underlap [53] have been explored. Moreover, several new structures incorporating 2D materials have been reported recently [50, 51, 54, 55, 56, 57]. For example, in [50], researchers introduced an n-p-n bipolar junction transistor (BJT) device composed of heavily doped molybdenum ditelluride (n-$MoTe_2$) and germanium selenide (p-GeSe). Additionally, in [51], a high gate-tunable rectification was demonstrated in a van der Waals heterostructure made from n-type rhenium disulfide (n-ReS2) and p-type germanium selenide (p-GeSe). Two-dimensional (2D) materials, such as graphene, transition metal dichalcogenides (TMDs), and black phosphorus, have emerged as promising candidates for the fabrication of T-CNTFETs. Their unique electronic properties, thinness, and high surface area offer significant advantages in the development of next-generation transistors.

In this work, we have proposed a novel doping-less transistor that incorporates drain work function engineering. The design features a zigzag-type CNT with a 1 nm diameter, utilizing HfO_2 as the gate oxide, which has a thickness of 2 nm and a dielectric constant of 16. The CNT remains intrinsic and serves as the semiconductor for both the source and drain regions, which are composed of metals with suitable work functions. In our proposed structure, the drain electrode is

segmented into two distinct sections, each measuring 15 nm in length and possessing different work functions (DWFs). The work function of the drain section adjacent to the channel (DWFAC) is set at 3.9 eV, which is 0.5 eV lower than that of the CNT. Meanwhile, the work function of the other part of the drain is chosen to be 3.4 eV, representing a 1 eV reduction relative to the CNT work function. All the techniques discussed in the literature aimed at enhancing the ON/OFF current ratio and minimizing ambipolarity in T-CNTFETs primarily influence the ON current performance, and gate-drain capacitance and often involve costly fabrication processes. The ambipolarity in T-CNTFET is owing to the undesired tunneling process at the drain-channel interface when the applied voltage at the gate is reversed. In our proposed structure, by using dual drain metals with different work functions, the tunneling barrier at the interface of the drain-channel is expanded, as a result, the ambipolar conduction and switching characteristics are improved. We have designated this innovative structure as the doping-less tunneling carbon nanotube field-effect transistor with dual different work functions in the drain region (DD-DL-TCNTFET). We conducted a comparative analysis between the proposed structure, the doping-less tunneling carbon nanotube field-effect transistor (DL-TCNTFET) [41], and the conventional tunneling carbon nanotube field-effect transistor (T-CNTFET) [12], all maintaining identical dimensions. Our simulations were executed in the ballistic regime, utilizing non-equilibrium Green's function (NEGF) analysis in mode-space to evaluate performance metrics and operational characteristics. This approach allows for a thorough understanding of how the modifications in the proposed DD-DL-TCNTFET influence its effectiveness compared to traditional designs. We utilized MATLAB 2019a software to analyze the proposed structure and plotted various performance parameter graphs. The simulation results indicate that the proposed DD-DL-TCNTFET significantly reduces the OFF-state current while enhancing the ON/OFF current ratio. Furthermore, the new structure exhibits enhanced ambipolarity, superior switching characteristics, and significantly reduced leakage current, effectively tackling two critical challenges commonly encountered in conventional T-CNTFETs.

The subsequent sections of the paper are organized as follows.

- Section 2 outlines the proposed device configuration and its physical characteristics.
- Section 3 details the simulation approach employed in our analysis.
- Section 4 presents the simulation results for the proposed structure.
- Section 5 compares the performance parameters of our structure with those of other recently reported devices.
- Sections 6 and 7 of the paper include perspectives, future trends, and a summary of findings and results.

2. Device configuration

Figure 1a,b illustrate the three-dimensional (3D) structure and a cross-sectional view of the proposed design. The nanotube employed is a zigzag type (13, 0) with a diameter of 1 nm. The gate oxide is composed of material HfO_2, featuring a thickness of 2 nm and a dielectric constant of 16. In the proposed structure, the drain electrode is partitioned into two segments, each 15 nm long (L_{D1} = 15 nm, L_{D2} = 15 nm), featuring different work functions (φ_{M3} and φ_{M4}). The work function of the drain section adjacent to the channel (φ_{M4}) is set at 3.9 eV, which is 0.5 eV lower than that of the CNT (φ_{M1} = 4.4 eV). The work function of the other portion of the drain (φ_{M3}) is set at 3.4 eV, representing a 1 eV decrease relative to the CNT work function. The source work function (φ_{M2}) is chosen as 5.4 eV, which is 1 eV higher than the CNT work function.

The lengths of both the drain and source are 30 nm ($L_D = L_S$ = 30 nm), while the gate length, equal to the channel length, is 20 nm (L_G = 20 nm), with no overlap between the source and drain. All simulations were conducted at a temperature of 300 K (T = 300 K) to demonstrate the performance enhancements of the proposed structure. We compared the DD-DL-TCNTFET with the DL-TCNTFET [41] and the conventional T-CNTFET [12] under identical dimensions and conditions. The simulations were performed in the ballistic regime employing non-equilibrium Green's function (NEGF) analysis in mode-space. All results presented here were obtained using MATLAB 2019a software. The physical details and specifications of the mentioned structures are summarized in Table 1.

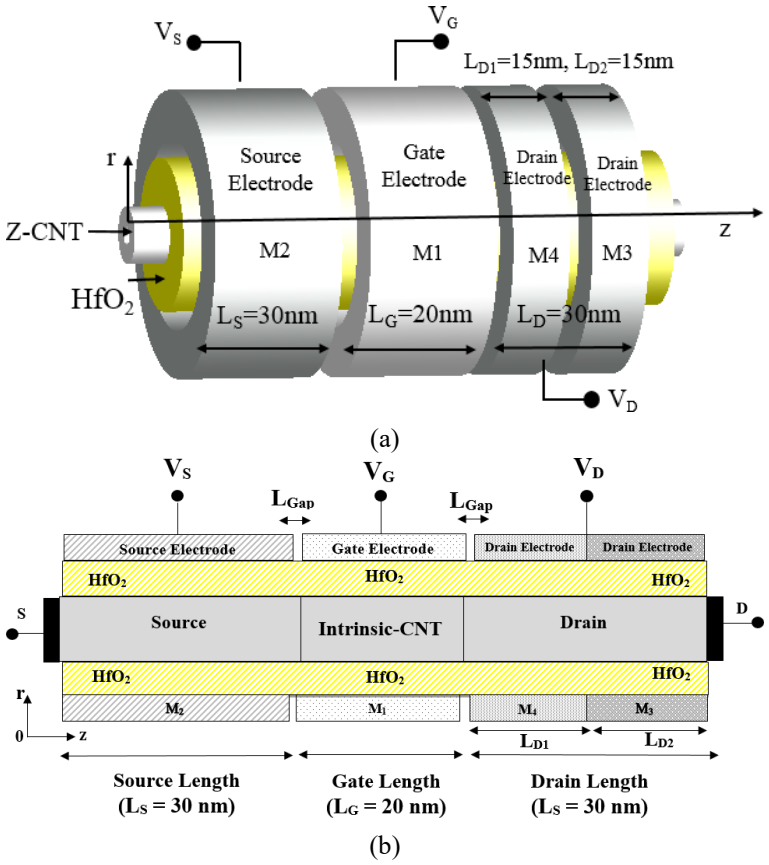


Figure 1. (**a**) Three-dimensional structure of the proposed design (DD-DL-TCNTFET). (**b**) Cross-sectional view of the DD-DL-TCNTFET, illustrating the arrangement of components, including the zigzag carbon nanotube, gate dielectric, and the dual work-function drain electrodes

Table 1. Details of physical characteristics of T-CNTFET [12], DL-TCNTFET [41], and DD-DL-TCNTFET structures

Parameters	Device Type		
	T-CNTFET [12]	DL-TCNTFET [41]	DD-DL-TCNTFET (Proposed)
CNT type	zigzag (13,0)	zigzag (13,0)	zigzag (13,0)
CNT diameter	1 nm	1 nm	1 nm
Gate length	20 nm	20 nm	20 nm
Drain length	30 nm	30 nm	L_{D1} = 15 nm, L_{D2} = 15 nm
Source length	30 nm	30 nm	30 nm
Gate dielectric constant	16	16	16
Gate dielectric thickness	2 nm	2 nm	2 nm
Temperature	300 K	300 K	300 K
Gate metal work function	4.4 eV	4.4 eV	φ_{M1} = 4.4 eV
Drain metal work function	-	3.4 eV	φ_{M4} = 3.9 eV, φ_{M3} = 3.4 eV
Source metal work function	-	5.4 eV	φ_{M2} = 5.4 eV
Source/drain doping density	1×10^7 cm^{-1}	-	-

From a fabrication standpoint, the development of an array of these nanodevices is expected to be highly beneficial, as it allows for the uniform production of individual devices without requiring junctions or variations in doping concentration. This simplification can enhance manufacturing efficiency and reduce costs. The fabrication possibility of the proposed structure based on the reports presented in [28, 58, 59, 60, 61] is described as follows. The fabrication process of doping-less T-CNTFETs begins with substrate preparation, where a clean silicon or silicon dioxide wafer is prepared for subsequent layers. CNTs are grown using chemical vapor deposition (CVD), allowing for control over their properties such as diameter and density. After growth, CNTs are transferred and aligned on the substrate. Source and drain electrodes are then formed by depositing metallic films through techniques such as photolithography or electron-beam lithography, followed by

creating a gate oxide layer made of high-k dielectric materials such as HfO_2 to regulate the electrostatic field in the channel. Subsequent steps involve precise etching to define the CNT channel length and ensure a doping-less structure without introducing doping profiles. Post-fabrication treatments, including thermal annealing, enhance contact quality between the CNTs and metal electrodes. Finally, the devices undergo electrical and structural testing to assess performance characteristics such as current-voltage behavior. For more details, refer to [28, 58, 59, 60, 61].

3. Simulation approach

In this paper, we present a numerical model of the Schrödinger equation utilizing the NEGF approach, applied self-consistently with the Poisson equation. The CNT channel, along with its coupling to the drain and source regions, is described through the Hamiltonian (H) matrix and corresponding self-energy matrices, denoted as $\sum_1$ and $\sum_2$. The Green's function is obtained by Equation (1) as outlined below [4, 7, 14, 16]:

$$G(E) = [(E + i\alpha^+)I - H - \sum\nolimits_1 - \sum\nolimits_2]^{-1} \tag{1}$$

In the equation above, E is energy level, α^+ is an infinitesimal value and I is the identity matrix. Once the Green's function is derived, various physical parameters can be obtained through the NEGF formulation. In the ballistic regime, the channel states are populated by the Fermi energy levels of the source and drain, determined by the equation [4, 7, 15, 17]:

$$D_{1(2)} = G\Gamma_{1(2)}G^{\dagger} \tag{2}$$

In the given expression, $G^{\dagger}$ corresponds to the Hermitian conjugate of matrix G, while $\Gamma_{1(2)}$ denotes the widening of energy levels resulting from the connections to the source and drain, as specified in Equation (3) [4, 7, 17]:

$$\Gamma_{1,2} = i(\sum\nolimits_{1,2} - \sum\nolimits^{\dagger}{}_{1,2}) \tag{3}$$

In the equation above, $\Sigma^{\dagger}$ is the Hermitean conjugate of the self-energy matrix. Next, the charge distribution within the channel is determined based on the states filled by the source and drain connections. The charge density in the CNT channel, utilizing the Green's function, can be expressed as [4, 7, 15, 17]:

$$\begin{aligned} Q(z) = (-e)\int_{-\infty}^{+\infty} dE \cdot \mathrm{sgn}[E - E_N(z)] \cdot \{D_S(E,z) \cdot f(\mathrm{sgn}[E - E_N(z)](E - E_{FS})) \\ + D_D(E,z) \cdot f(\mathrm{sgn}[E - E_N(z)](E - E_{FD}))\} \end{aligned} \tag{4}$$

where, e is the electron charge, E_N is the neutral charge level, sgn(E) is the sign function, f is the Fermi-Dirac distribution function, D_S and D_D are the local densities of states for the source and drain, E_{FS} and E_{FD} are the Fermi level of the source and drain, respectively. To achieve a self-consistent solution, the NEGF equation is iteratively solved alongside the Poisson equation until convergence is reached. After establishing self-consistency, the source-drain current can be computed by use of the Landauer—Buttiker formula according to the Equation (5) as follows [4, 7, 17]:

$$I = \frac{4e}{h}\int T(E)[f_1(E) - f_2(E)]dE \tag{5}$$

where, h represents Planck's constant and $T(E)$ is the transmission coefficient, computed as follows [4, 7, 17]:

$$T(E) = \mathrm{Tr}(\Gamma_1 G \Gamma_2 G^{\dagger}) \tag{6}$$

where, *Tr* is the trace operator. Overview of simulation algorithm and iteration process in NEGF analysis illustrates in Figure 2. For the digitization and numerical modeling of the device structure in two dimensions, mesh sizes are set to 0.25 nm in the Z-direction and 0.1 nm in the R direction, both selected uniformly. Moreover, for the simulation of the DD-DL-TCNTFET, DL-TCNTFET, and conventional T-CNTFET, we employed the self-consistent coupling of Poisson and Schrödinger equations within the NEGF framework. All simulation outcomes were generated using MATLAB 2019.a, with the accuracy of the simulator confirmed in prior studies [12, 16, 17, 22, 24].

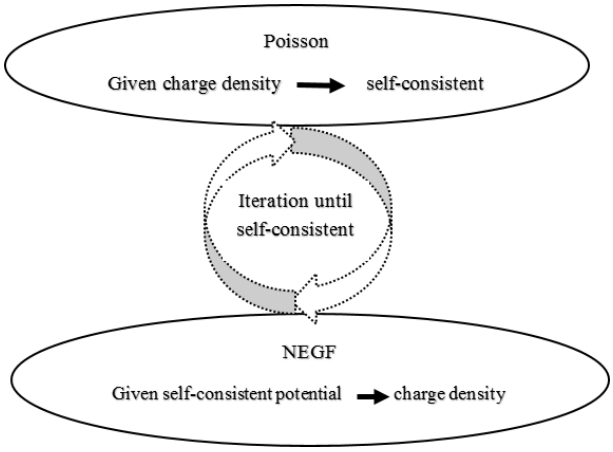


Figure 2. Overview of simulation algorithm and iteration process in NEGF analysis

4. Simulation results and discussions

Figure 3a presents the transport characteristics of the proposed structure (DD-DL-TCNTFET), DL-TCNTFET, and the conventional T-CNTFET, evaluated under two distinct drain-source voltages. The results indicate that DD-DL-TCNTFET significantly decreases the OFF state current when compared to both the DL-TCNTFET and conventional T-CNTFET structures. Additionally, there is a notable improvement in ambipolarity, enhancing the device's versatility and performance in various applications.

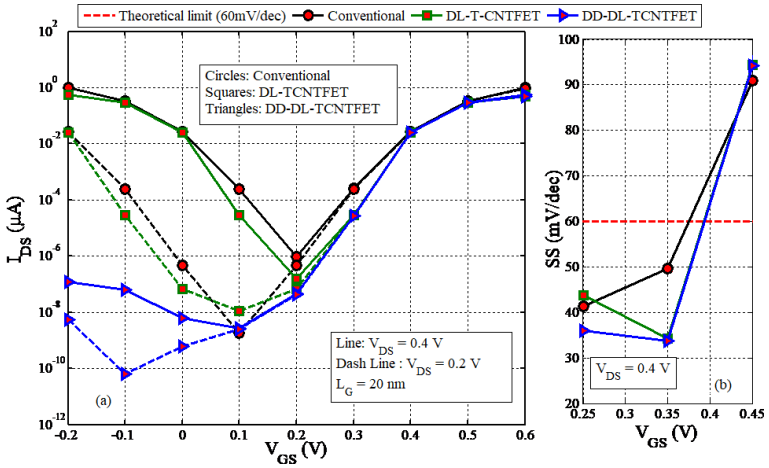


Figure 3. (**a**) I_{DS}-V_{GS} transfer characteristics diagram in V_{DS} = 0.2, 0.4 V (**b**) sub-threshold swing versus gate-source voltage in V_{DS} = 0.4 V

In the proposed structure utilizing dual drain electrodes with DWFs, the tunneling barrier at the drain-channel interface is effectively widened, resulting in a reduced probability of band-to-band tunneling (BTBT). As a result, the OFF state current for the proposed design at V_{DS} = 0.2 V and V_{GS} = 0 V is approximately six times smaller than that of both the DL-TCNTFET and the conventional T-CNTFET.

The sub-threshold slope is critical phenomena in examining SCEs. A greater value of this slope indicates that the device is more reliable and exhibits lower leakage currents, thereby reducing the sub-threshold swing (SS). The SS parameter is essential for assessing power consumption in the sub-threshold region of short-channel devices. Conventional TCNTFETs achieve a sub-threshold swing that is smaller than the theoretical limit of 60 mV/decade, making these devices particularly attractive for low-power dissipation applications. The sub-threshold swing can be determined using the following formula [15, 17]:

$$SS = 10^3 \frac{V_{GS2} - V_{GS1}}{\log(I_{DS2}) - \log(I_{DS1})} (\text{mV/dec}) \tag{7}$$

In Figure 3b, the sub-threshold swing (SS) is analyzed as a function of gate-source voltage. The results indicate that the proposed structure demonstrates a significant improvement in sub-threshold swing compared to the other two mentioned structures. Specifically, at V_{DS} = 0.4 V and V_{GS} = 0.3 V, the proposed structure achieves an SS of 34.82 mV/decade, while the DL-TCNTFET exhibits an SS of 38.97 mV/decade, and the conventional T-CNTFET shows an SS of 45.45 mV/decade. The reduction in SS in the proposed design can be attributed to the widening of the tunneling barrier at the drain-channel interface, facilitated by the dual electrodes with DWFs in the drain region. This enhancement improves the tunneling phenomenon and the ambipolarity of the device. As a result, the electrostatic control capability of the gate is increased, leading to a more favorable distribution of the central potential within the channel, and ultimately reducing SCEs.

Drain current versus of the drain-source voltage for the DD-DL-TCNTFET, DL-TCNTFET, and conventional T-CNTFET is presented in Figure 4. According to the figure, the saturation current of both the proposed structure and the DL-TCNTFET is lower than that of the conventional T-CNTFET across the specified gate-source voltages. Specifically, at a gate-source voltage of V_{GS} = 0.5 V, the ON state current for the proposed structure and the DL-TCNTFET is 0.29 µA, while the conventional T-CNTFET shows an ON state current of 0.33 µA.

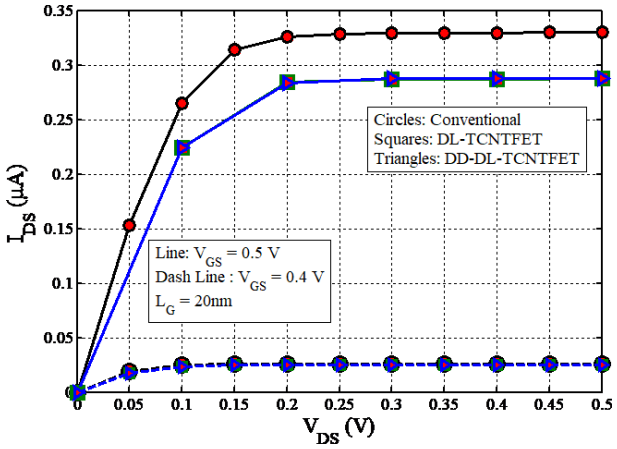


Figure 4. Drain current versus of the drain-source voltage for T-CNTFET, DL-TCNTFET and DD-DL-TCNTFET structures in V_{GS} = 0.4, 0.5 V

Figure 5 depicts the ON/OFF current ratio as a function of the ON state current. This current ratio is obtained from the transfer curve in Figure 3a by horizontally sweeping a window of V_{DD}, defined between V_{GS-ON} and V_{GS-OFF} (where $V_{GS-OFF} = V_{GS-ON} - V_{DD}$), corresponding to I_{ON} and I_{OFF}, respectively. The power supply voltage is set to 0.4 V (V_{DD} = 0.4 V).

As observed, the current ratio at V_{DS} = 0.4 V for DD-DL-TCNTFET is higher than that of both the DL-TCNTFET and conventional T-CNTFET structures. The maximum current ratio for the DD-DL-TCNTFET exceeds 10^8, while the ratios for the DL-TCNTFET and conventional T-CNTFET are on the order of 10^6. The significant improvement in the current ratio of the DD-DL-TCNTFET structure can be attributed to the reduced curvature of the energy band near the drain-channel interface and the narrowing of the tunneling path in the OFF state.

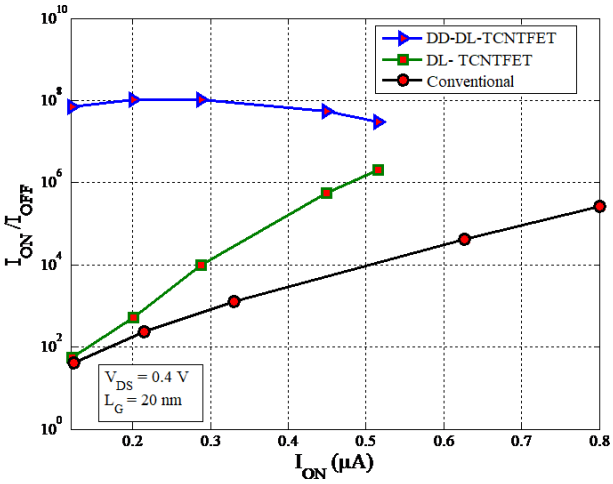
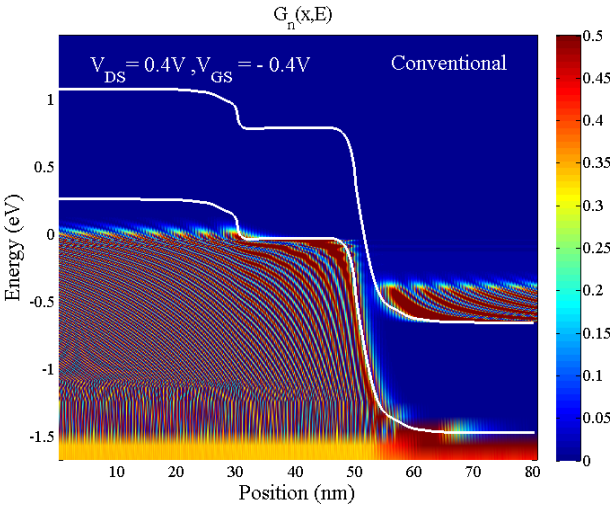


Figure 5. The ON/OFF current ratio curve versus ON current for the DD-DL-TCNTFET, DL-TCNTFET and conventional structures in V_{DS} = 0.4 V

Figure 6 presents the energy band diagram as a function of position along the CNT channel for the mentioned structures at V_{GS} = −0.4 V and V_{DS} = 0.4 V. As indicated in Figure 6, the separation between the conduction and valence bands at the channel-drain interface for the proposed structure is greater than that observed in the other two structures. As a result, the probability of BTBT in DD-DL-TCNTFET at negative gate-source voltages is significantly lower. The DD-DL-TCNTFET structure, which incorporates dual electrodes with DWFs along the drain region, effectively reduces the curvature of the energy band in proximity to the drain-channel junction. This results in a wider tunneling barrier and enhances the ambipolarity compared to the other two structures.



(a)

Figure 6. *Cont.*

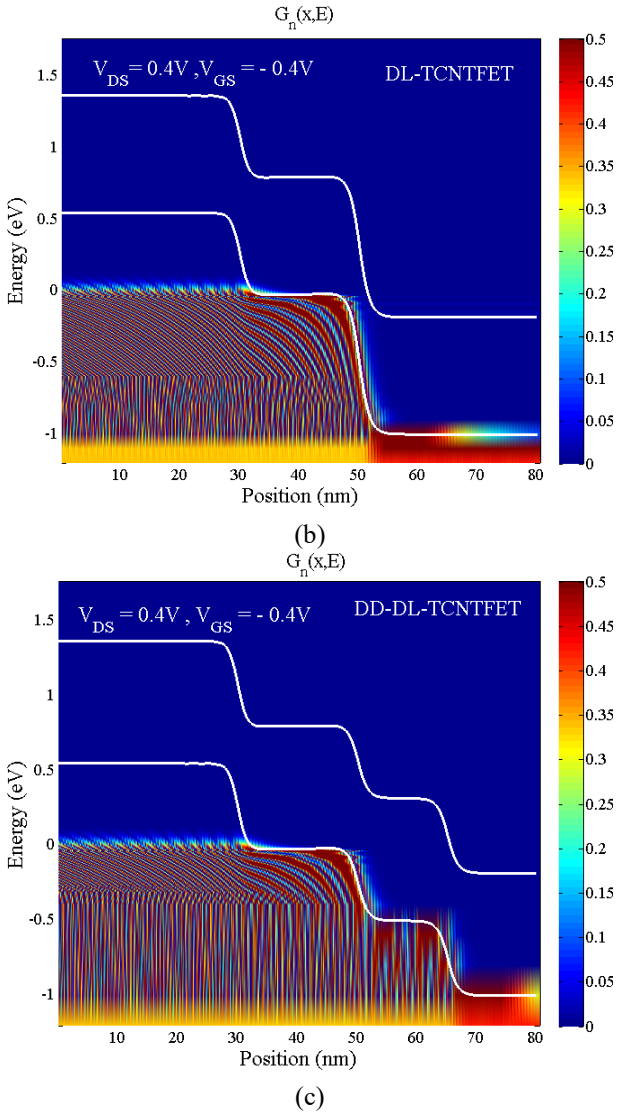


Figure 6. Energy band diagrams versus position along the CNT channel for the structures (**a**) conventional T-CNTFET (**b**) DL-TCNTFET and (**c**) DD-DL-TCNTFET, illustrating the tunneling width between the channel's valence band and the drain's conduction band at V_{DS} = 0.4 V and V_{GS} = −0.4 V

Figure 7 illustrates the magnitudes of the electric field as a function of position along the CNT. It is notable that the maximum electric field in the ON state is reduced in DD-DL-TCNTFET compared to both the DL-TCNTFET and conventional T-CNTFET structures. This reduction effectively mitigates the effects of hot carriers, which are unfavorable and potentially detrimental phenomena in short-channel devices. Consequently, the proposed design demonstrates enhanced reliability by limiting the impact of hot carrier effects.

4.1 *Influence of variations in the lengths of the drain electrodes on the ON/OFF current ratio*

In this section, we aimed to further explore and assess the proposed structure by analyzing how variations in the lengths of the drain electrodes (L_{D1}, L_{D2}) impact the device's performance, while keeping the work functions constant (φ_{M3}, φ_{M4}). Initially, we set the lengths of the drain electrodes equal (L_{D1} = L_{D2} = 15 nm). We then varied the lengths of the drain electrodes to L_{D1} = 5 nm, L_{D2} = 25 nm; L_{D1} = 10 nm, L_{D2} = 20 nm; L_{D1} = 15 nm, L_{D2} = 15 nm; L_{D1} = 20 nm, L_{D2} = 10 nm; and L_{D1} = 25 nm, L_{D2} = 5 nm, conducting the necessary investigations for each case. Figure 8 illustrates the

transfer characteristics of the proposed structure. It was observed that as the length of L_{D1} increases, the OFF state current decreases, indicating that the tunneling barrier at the channel-drain interface widens, which improves ambipolarity.

Figure 9 illustrates the ON/OFF current ratio in relation to the ON current as the length of L_{D1} is varied in the proposed structure at V_{DS} = 0.4 V. The data shows that reducing the OFF-state current leads to a significant increase in the ON/OFF current ratio within the proposed structure. As L_{D1}'s length increases, the current ratio improves owing to a reduced band curvature in proximity to the drain-channel junction which shortens the tunneling path in the OFF state. Notably, while the leakage current associated with L_{D1} decreases substantially with increasing length, the ON current also experiences a slight reduction. Consequently, we chose to set the lengths of the drain electrodes to 15 nm (L_{D1} = L_{D2} = 15 nm).

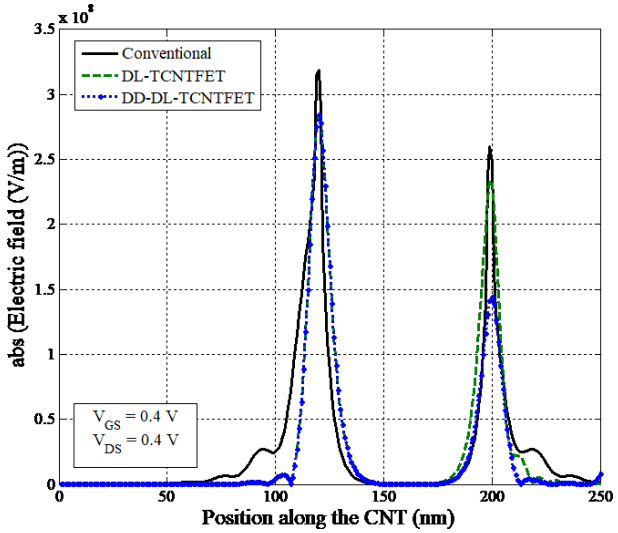


Figure 7. Electric field versus position along the CNT at V_{DS} = 0.4 V and V_{GS} = 0.4 V

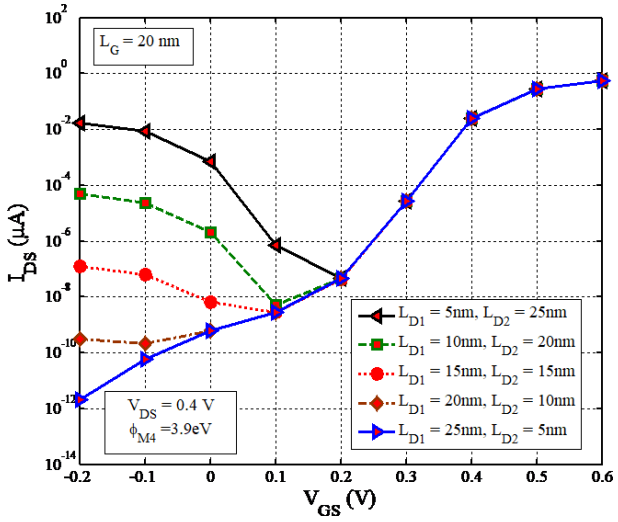


Figure 8. Transfer diagram by changing the length of L_{D1} in the proposed structure at V_{DS} = 0.4 V

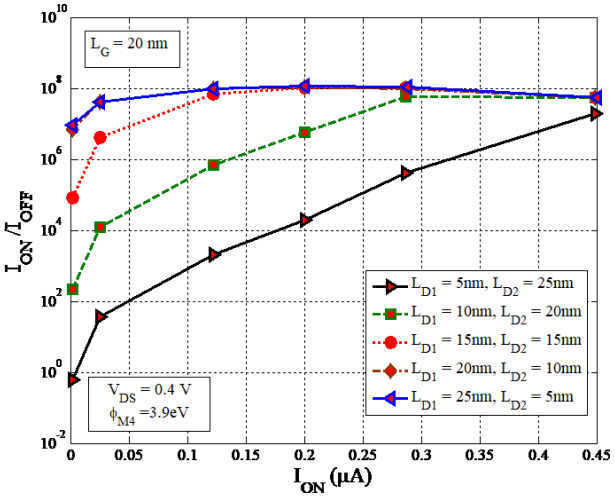


Figure 9. The ON/OFF current ratio versus ON current by changing the length of L_{D1} in the proposed structure at V_{DS} = 0.4 V

4.2 *Influence of increasing the work function of the drain section adjacent to the channel on the ON/OFF current ratio*

To further investigate and gather more precise data about the performance of the DD-DL-TCNTFET structure, we fixed the lengths of L_{D1} and L_{D2} at 15 nm and varied the DWFAC (φ_{M4}). We initially set the DWFAC at 3.9 eV and then selected φ_{M4} values of 3.6, 3.7, 3.8, 3.9, and 4 eV. The transfer characteristics and the ON/OFF current ratio for these configurations are illustrated in Figures 10 and 11, respectively. It is evident that as φ_{M4} is adjusted from 3.6 eV to 4 eV, the OFF state current decreases while the current ratio increases, as demonstrated in Figure 11. It is important to note that there are limitations to increasing the value of the DWFAC (φ_{M4}), as doing so can misalign the energy bands at the channel-drain interface. This misalignment leads to an increased tunneling barrier in the channel-drain region, which poses an obstacle for charge carriers attempting to cross from the channel to the drain in the ON state. Consequently, while increasing φ_{M4} may reduce the OFF state current and improve the ON/OFF current ratio, it also results in a decrease in the ON current. Therefore, a trade-off must be carefully considered between the value of φ_{M4}, the ON state current, and the leakage current to optimize the overall performance of the proposed structure.

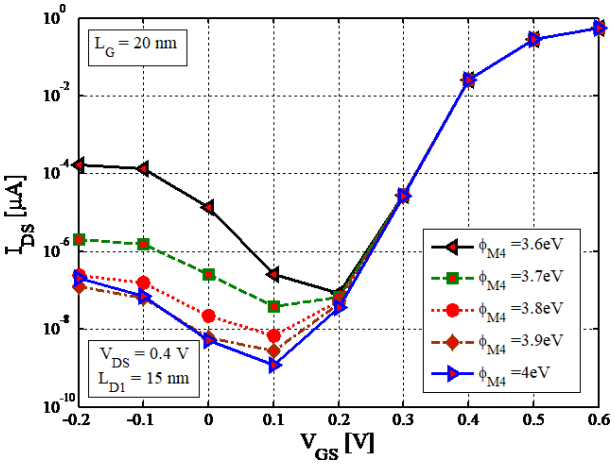


Figure 10. Transfer diagram by changing the φ_{M4} in the proposed structure at V_{DS} = 0.4 V

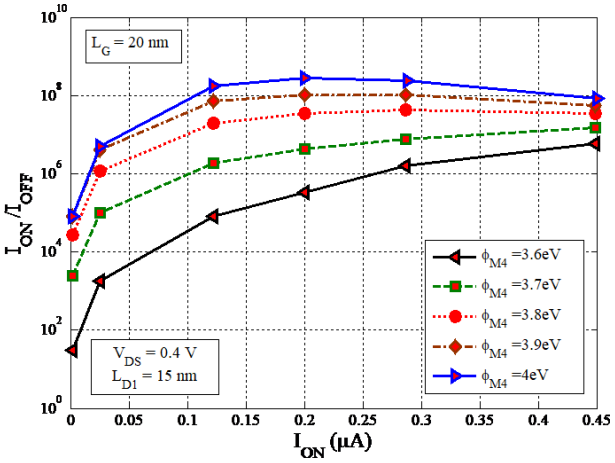


Figure 11. The ON/OFF current ratio versus ON current by changing the φ_{M4} in the proposed structure at V_{DS} = 0.4 V

Figures 12 and 13 illustrate the sub-threshold swing and the current ratio as functions of the DWFAC (φ_{M4}) and the length of L_{D1}. The simulation results show that, within the defined range, as both φ_{M4} and L_{D1} increase, the SS parameter exhibits a decreasing trend, while the current ratio demonstrates an increasing trend. The presence of dual drain electrodes with DWFs in the proposed structure effectively increases the channel length owing to the widening of the barrier. This expansion leads to a reduction in leakage current, which in turn contributes to a lower SS. A smaller SS enhances channel control, reduces leakage, and minimizes energy dispersion, leading to an improved I_{ON}/I_{OFF} ratio and better scalability for the device. Consequently, this design approach improves the overall device performance by enhancing the current ratio and optimizing the switching characteristics.

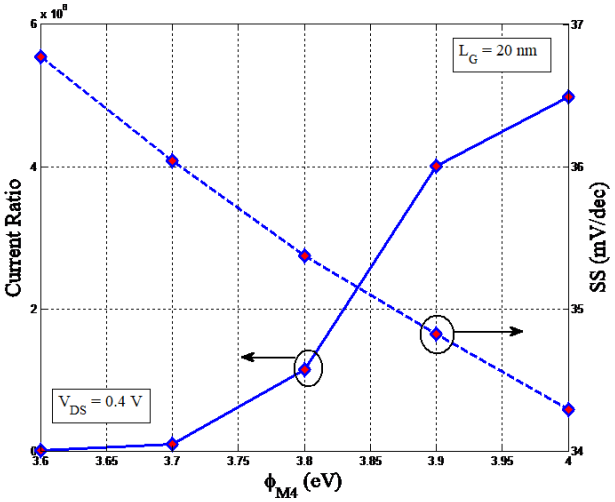


Figure 12. Current ratio diagram and sub-threshold swing versus φ_{M4} in V_{DS} = 0.4 V

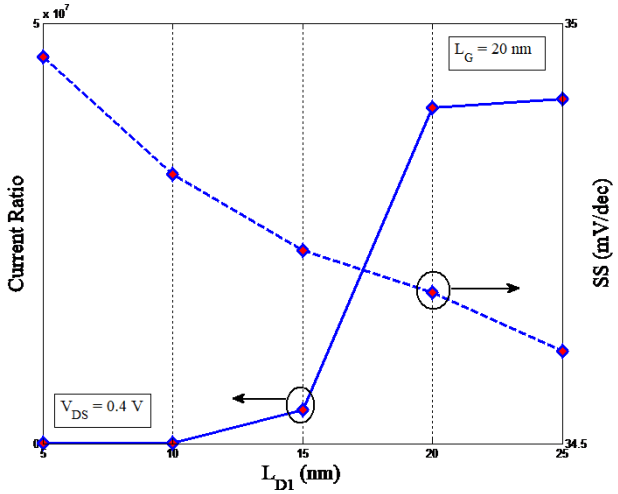


Figure 13. Current ratio diagram and sub-threshold swing versus the length of L_{D1} in V_{DS} = 0.4 V

5. The proposed structure performance comparisons

To evaluate the advantages of the proposed design in the nanoscale regime, we performed a quantum simulation-based comparison among DD-DL-TCNTFET, DL-TCNTFET, and conventional T-CNTFET structures, focusing on key performance parameters. Table 2 presents the comparative results for these structures. The findings indicate that the ON/OFF current ratio has improved by approximately five orders of magnitude, with a sub-threshold swing recorded at 34.82 mV/dec in the nanoscale regime. Furthermore, both the OFF current and leakage current have decreased significantly, which is particularly beneficial for high-speed, low-power consumption, and superior-performance switching applications. These improvements highlight the efficacy of the proposed design in enhancing device performance in nanoscale electronics.

Table 2. Comparison of several key parameters of the proposed structure, DL-TCNTFET, and the conventional T-CNTFET structures

Parameters	Structures		
	Conventional	DL-TCNTFET	DD-DL-TCNTFET
ON current (μA)	3.30×10^{-1}	2.87×10^{-1}	2.88×10^{-1}
OFF current (μA)	2.50×10^{-4}	2.96×10^{-5}	2.74×10^{-9}
ON/OFF current ratio	1.30×10^{3}	9.72×10^{3}	1.05×10^{8}
Subthreshold swing (mV/dec)	45.45	38.97	34.82

Moreover, a comparison has been conducted between several parameters of the proposed structure and those of previously reported architectures, as summarized in Table 3. The results indicate that the ON/OFF current ratio and SS values of DD-DL-TCNTFET outperform many of the structures documented in the literature. Significantly, the ambipolarity observed in the proposed device has been greatly reduced and is nearly eliminated. This enhancement is attributed to the optimization of the DWFAC (φ_{M4}) and the length of L_{D1}, tailored for the desired performance.

Additionally, one of the challenges commonly associated with CNTFET structures pertains to doping control at the junctions between n-type and p-type regions or their intrinsic counterparts. In our proposed structure, which leverages DL technology, the need for doping has been eliminated, effectively resolving this issue. This advancement not only simplifies fabrication but also contributes to the overall performance and reliability of the device. Additionally, the process of importing doping and establishing n-type to p-type connections, as well as working with intrinsic materials, necessitates highly advanced and precise equipment. This remains a significant challenge, particularly at very small scales.

Based on the studies conducted on the proposed structure, it can be concluded that the dual drain electrodes with DWFs and a length of $L_{D1} = L_{D2} = 15$ nm demonstrate superior performance. This configuration results in notable

improvements in several key metrics, including transfer characteristics, sub-threshold swing, ON/OFF current ratio, reduction of ambipolarity, and decreased leakage current. These enhancements underscore the effectiveness of the proposed design in advancing CNTFET technology for nanoscale applications.

Table 3. Comparison of the sub-threshold swing and the ON-OFF current ratio of different structures for TFETs

Types of TFET Structures	Simulation Approach	Ref.	Parameters		
			Sub-Threshold Swing (mV/dec)	ON/OFF Current Ratio	VDD(V)
N-N+-N FET	NEGF	[46]	92	7×10^3	0.5
MDDP-T-CNTFET	NEGF	[16]	36.66	3.66×10^2	0.4
U-CNTFET	NEGF	[45]	66	2.8×10^3	0.4
P-N TFET	NEGF	[42]	60	2×10^3	0.3
DL-TCNTFET	NEGF	[41]	38.97	9.72×10^3	0.4
DJSD-DL-CNTFET	NEGF	[37]	59.67	1.12×10^5	0.3
Proposed (DD-DL-TCNTFET)	NEGF	-	34.82	1.05×10^8	0.4

6. Perspectives and future trends

Two-dimensional materials, such as graphene, transition metal dichalcogenides (TMDs), and black phosphorus, have emerged as promising candidates for the fabrication of T-CNTFETs. Their unique electronic properties, thinness, and high surface area offer significant advantages in the development of next-generation transistors [54, 55]. Many 2D materials exhibit excellent carrier mobility, which can lead to enhanced switching speeds and improved overall device performance in TFETs. This is especially beneficial for high-frequency applications. The ability to tune the band gap of 2D materials through layer thickness adjustments or chemical modification enables precise control over the electronic properties of TFETs, allowing for optimized performance in specific applications. TFETs constructed with 2D materials can operate at lower voltage levels compared to traditional MOSFETs. This characteristic is crucial for low-power electronics, extending battery life in portable devices [56, 57]. Many 2D materials can exhibit ambipolar transport properties, allowing for both n-type and p-type behavior. This versatility can be leveraged in the design of mixed-signal circuits and complementary logic devices. The 2D nature of these materials allows for the fabrication of ultrathin devices, reducing SCEs and improving scalability for future nanoscale applications. The integration of 2D materials in tunneling FETs presents exciting opportunities to overcome the limitations of conventional semiconductor technologies. With their unique properties enabling low-power operation, high-speed performance, and versatility, 2D materials are set to play a significant role in the development of next-generation electronic devices and systems [54, 55, 56, 57]. Ongoing research and innovation in this field continue to unveil their vast potential in both academic and industrial applications. This presents a highly appealing opportunity to advance both theoretical and practical studies in the future. This issue may be studied in the future works of our research group.

7. Conclusions

In this paper, we propose a novel structure based on a DL-T-CNTFET utilizing work function engineering. The electrical properties of the device are simulated using the NEGF approach. A comparative analysis was conducted between the proposed structure, the DL-T-CNTFET, and the conventional T-CNTFET, all maintaining the same dimensions. The results demonstrate that the proposed structure exhibits superior immunity against SCEs owing to the application of drain work function engineering. By employing two electrodes with distinct work functions in the drain region, the curvature of the energy bands near the drain-channel interface is reduced, resulting in a wider tunneling barrier compared to the other two structures. Additionally, the proposed design offers several advantages, including a high ON/OFF current ratio, a lower sub-threshold swing, and a reduced ON-state electric field. These enhancements indicate the potential of the proposed DL-T-CNTFET structure for improved performance in nanoscale electronic applications.

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Data availability

The data will be available if requested.

Conflict of interest

The authors declare that there are no conflict of interest.

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