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Research Article

Modeling, Control, and Simulation of a Common-Emitter Switched Amplifier with a Voltage-Variable Gain

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Abstract: A novel topology of a switched amplifier configured as a common-emitter voltage variable gain amplifier, along with the implementation of a control system aimed at regulating the output voltage is introduced in this article. A key focus of this work is addressing the challenge of output voltage regulation in the presence of variations in voltage gain caused by changes in the output load. The proposed topology integrates a standard common-emitter amplifier with an additional switch connected to the emitter terminal, which enables implementing an efficient control over the amplifier's voltage gain. The feasibility and operation of the presented system are satisfactorily evaluated through simulation studies.

Keywords: BJT, hysteresis controller, non-linear model, OP-AMP, switched amplifier

1. Introduction

One of the central topics in the domain of microelectronics is the theory and design of low-power signal amplification, an area that has garnered extensive research attention due to its widespread applications in modern electronic systems [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14]. Bipolar junction transistors (BJTs) and operational amplifiers (OP-Amps) are the most commonly utilized components for signal amplification within this field, with OP-Amps being particularly prominent across a broad frequency spectrum [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14]. Conversely, field-effect transistors (FETs), such as junction field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), are primarily employed in switching applications [15] and are less frequently integrated into traditional amplifier circuits.

OP-Amps have become the preferred choice for medium-frequency voltage amplification due to their performance and versatility, whereas the use of BJTs for such applications has significantly declined, especially for low- and medium-frequency amplification tasks [16, 17]. In these applications, OP-Amps are typically employed without active regulation of the amplification mechanisms, which rely primarily on the passive resistors in the biasing circuitry [16, 17]. In contrast, BJTs offer a direct relationship between the output gain and the load resistor R_L, which introduces challenges in maintaining stable and consistent output voltage due to fluctuations or disturbances in R_L, thereby complicating control and regulation.

To overcome the inherent limitations associated with the load-resistor-dependent gain in BJT-based amplifiers, this work proposes the application of a fundamental control theory concept: the implementation of a feedback loop. By comparing the output voltage with a reference signal, an error signal is generated, which is subsequently processed by a compensator or controller. The controller's output then adjusts the actuator, enabling the amplifier to maintain the desired

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output characteristics despite fluctuations in the system or external disturbances [18, 19]. This feedback approach is crucial for enhancing the precision and stability of the amplifier's operation, ensuring a more controlled amplification process.

The core contribution of this work is the development of a novel amplifier topology—the common-emitter switched amplifier (CE-SA)—with a variable and controllable voltage gain. This topology, designed to meet the demands for flexible and precise amplification in a range of applications, is detailed in Section 2. Following the introduction of the topology, Section 3 provides the dynamic modeling of the CE-SA, offering insights into its operational behavior across different conditions and allowing for a thorough analysis of its performance under varying parameters. Section 4 describes the proposed control strategy, while Section 5 showcases the simulation results that validate the effectiveness of the design. Section 6 presents a comparison with previous work, highlighting the innovations and advantages of the proposed design in relation to existing amplifier systems. Finally, Section 7 offers a comprehensive conclusion, summarizing the findings and implications of the study.

2. Proposed CE-SA topology

The proposed CE-SA topology, as illustrated in Figure 1, is based on a conventional common-emitter amplifier configuration [16, 17], wherein the bipolar junction transistor (BJT) Q_1 serves as the primary active amplifier element. In contrast, BJT Q_2 functions as the switching component, operating within the saturation and cutoff regions [16, 17]. This unique topology is further augmented by key passive components, including bias resistors R_1 and R_2, the collector resistor R_C, and the emitter resistor R_E, all of which contribute to the establishment of the biasing conditions for the amplifier. The bias voltage is defined as V_{CC}.

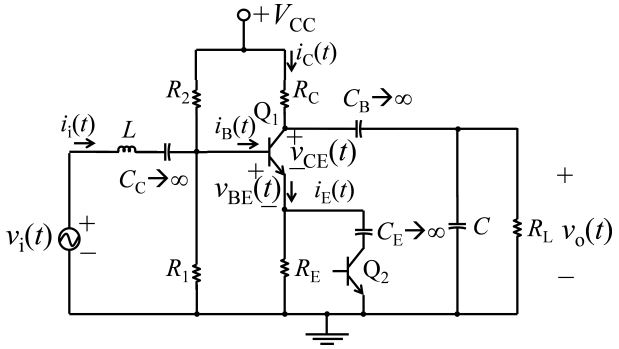

Figure 1. Proposed topology of CE-SA. Illustrates the configuration of the CE-SA, including the amplifier and switching elements, with key components such as coupling capacitors, inductors, and resistors

In the alternating current (AC) operating regime, the circuit is interfaced with an input stage consisting of a sinusoidal voltage source $v_i(t)$ and an inductor L, which acts as an input filter. A coupling capacitor (C_B) is used to connect the amplifier with the output stage, which is composed of an output filter capacitor C and the load resistor R_L. The pass capacitor C_E plays a pivotal role by coupling the switching transistor Q_2 into the circuit, enabling switched operation, thereby facilitating variable gain adjustment.

The circuit dynamics are characterized by the following current paths: $i_i(t)$ representing the input current, $i_C(t)$ the collector current, $i_B(t)$ the base current, and $i_E(t)$ the emitter current. Additionally, the voltages $v_{BE}(t)$ and $v_{CE}(t)$ denote the base-emitter and collector-emitter voltage drops, respectively, while $v_o(t)$ refers to the output voltage of the amplifier.

A key feature of this topology is the design of the coupling capacitors (C_C, C_B, and C_E), which are engineered to behave as short circuits within the medium-frequency range. In this operational range, the output capacitor and the input inductor function as reactive filters, ensuring effective signal filtering and impedance matching. These components, together with the active elements, create a robust and versatile amplifier system capable of delivering controlled voltage gain across a variety of applications.

3. Modeling of the CE-SA

In this section, the fundamental equations governing the CE-SA are presented, considering both the DC and AC operating conditions. It is assumed that transistor Q_1 operates in the linear region, ensuring accurate signal amplification [16, 17].

3.1 *DC operation*

In the DC operating regime, the coupling capacitors C_B, and C_E are treated as open circuits, resulting in the modified configuration shown in Figure 2a. This transforms the CE-SA into a standard DC-biased amplifier circuit. By combining resistors R_1 and R_2 with the DC supply voltage V_{CC}, a Thévenin equivalent circuit can be derived. The resulting circuit, tailored for DC operation, is shown in Figure 2b.

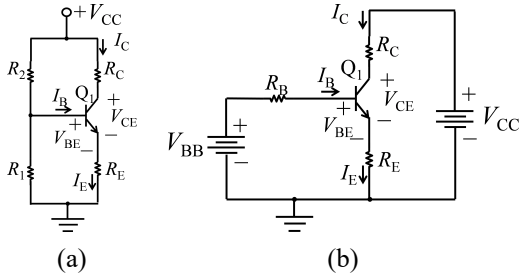

Figure 2. CE-SA operating in DC regime. (**a**) Topology of the CE-SA in DC bias. The capacitors C_B, C_C, and C_E approach open circuits; (**b**) Topology of the CE-SA in dc bias with equivalent Thévenin input network

To analyze this circuit, the Thévenin equivalent voltage V_{BB} and resistance R_B are expressed as:

$$V_{BB} = \frac{R_B}{R_2} \cdot V_{CC} \tag{1}$$

$$R_B = R_1 || R_2 \tag{2}$$

Here, $R_1 // R_2$ indicates the parallel combination of R_1 and R_2.

Using these parameters, the quiescent point of the amplifier can be determined. To maximize the output voltage swing, the collector-emitter voltage V_{CEQ} is set to:

$$V_{CE_Q} = \frac{1}{2} \cdot V_{CC} \tag{3}$$

The quiescent collector current I_{CQ} is given by:

$$I_{C_Q} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta} + R_E} \tag{4}$$

Here, β represents the current gain of the transistor [16], and V_{BE} is the base-emitter voltage, typically 0.7 V for silicon BJTs.

3.2 *AC operation*

For AC operation, the coupling capacitors C_B, C_C, and C_E are treated as short circuits, allowing the circuit to process time-varying signals. Transistor Q_1 is replaced with its small-signal model [16, 17], and Q_2 is modeled using a switching function $s(t)$, which represents its on/off state. The AC equivalent circuit is shown in Figure 3a.

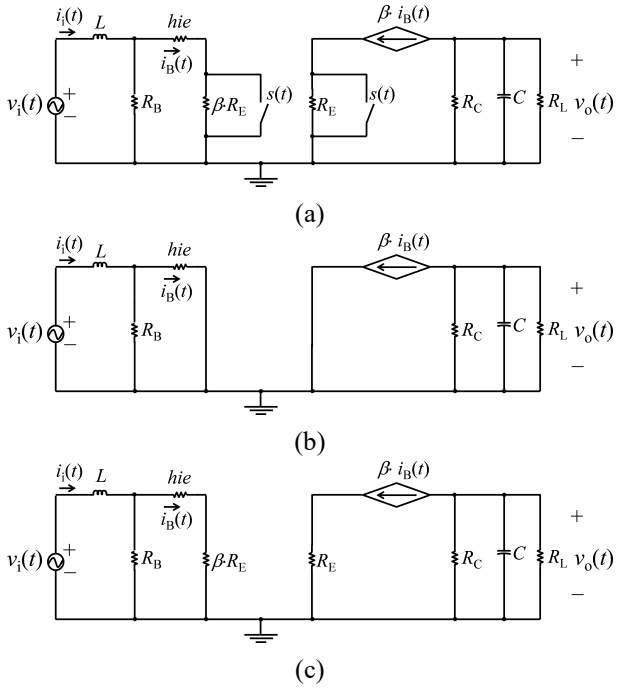

Figure 3. CE-SA switching model for AC regime operation. (**a**) CE-SA switching model with the incorporation of the reflection of R_E and the switching function $s(t)$; (**b**) CE-SA switching model when $s(t)$ is on; (**c**) CE-SA switching model when $s(t)$ is off

The switching function $s(t)$ is defined as follows:

$$s(t) = \begin{cases} 1, & \text{if } Q_2 \text{ is on (saturation region)} \\ 0, & \text{if } Q_2 \text{ is off (cutoff region)} \end{cases} \tag{5}$$

This switching behavior results in two distinct circuit configurations, depending on the state of Q_2.

When $s(t) = 1$, the bypass capacitor C_E shorts R_E, placing the system in the configuration shown in Figure 3b. The state-space equations for this configuration are in the following Equation (6). From here:

- *hie*: Input resistance of Q_1 in the common emitter configuration.

$$\frac{d}{dt}\begin{bmatrix} i_i(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_B \| hie}{L} & 0 \\ -\beta \cdot \frac{R_B \| hie}{hie \cdot C} & -\frac{1}{R_o \cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_i(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_i(t) \tag{6}$$

- R_o: Parallel combination of R_C and R_L, $R_o = R_C // R_L$.

Similarly, when $s(t) = 0$, R_E is active in the circuit, leading to the configuration shown in Figure 3c. The state-space equations are:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{L} & 0 \\ -\beta \cdot \frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}} \cdot C} & -\frac{1}{R_{\mathrm{o}} \cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{\mathrm{i}}(t) \tag{7}$$

where:

- $R_{\mathrm{i}} = hie + \beta \cdot R_{\mathrm{E}}$: Effective input resistance considering R_{E}.

The combined switching model is derived by integrating the equations for both states using $s(t)$ as the governing parameter.

This approach yields the general state-space representation as follows in (8).

To further aid in understanding, Figure 4 illustrates the equivalent switching model of the CE-SA. The constants appearing in the current-controlled voltage source and current-controlled current source are defined as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{(R_{\mathrm{i}}||R_{\mathrm{B}} + ((R_{\mathrm{B}}||hie) - (R_{\mathrm{i}}||R_{\mathrm{B}})) \cdot s(t))}{L} & 0 \\ -\frac{\beta \cdot \left(\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}} + \left(\left(\frac{R_{\mathrm{B}}||hie}{hie}\right) - \left(\frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}}\right)\right) \cdot s(t)\right)}{C} & -\frac{1}{R_{\mathrm{o}} \cdot C} \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{i}}(t) \\ v_{\mathrm{o}}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \cdot v_{\mathrm{i}}(t) \tag{8}$$

$$k_{11} = R_{\mathrm{B}}||hie - R_{\mathrm{i}}||R_{\mathrm{B}} \tag{9}$$

$$\begin{cases} k_{21} = \frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}} \\ k_{22} = \frac{R_{\mathrm{B}}||hie}{hie} - \frac{R_{\mathrm{i}}||R_{\mathrm{B}}}{R_{\mathrm{i}}} \end{cases} \tag{10}$$

Note that from (8), it is observed that the output $v_{\mathrm{o}}(t)$ shows a negative polarity, thereby confirming the inverting nature of this type of amplifiers in terms of voltage gain, $A_{\mathrm{v}} = v_{\mathrm{o}}(t)/v_{\mathrm{i}}(t)$ [16, 17].

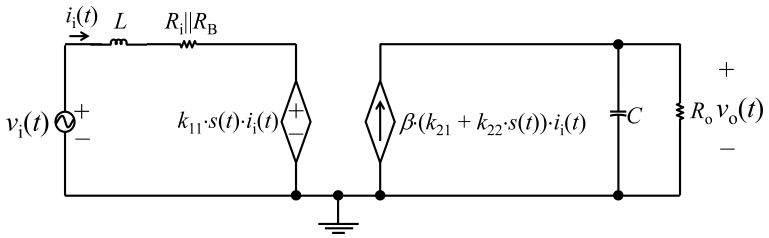

Figure 4. Switching model of the CE-SA. Shows the full switching model, including Q_2 and the switching transitions based on the error signal

4. Control strategy

The primary objective of the CE-SA control is to regulate the time-varying voltage gain A_{v}, ensuring controlled amplification of the system. This poses a significant challenge due to the nonlinearity and discreteness of the system dynamics, as evidenced by (8). Traditional linear control methods such as PI or PID controllers were considered; however, these techniques often struggle with highly nonlinear systems, particularly when rapid transitions and a high degree of precision are required [20, 21, 22, 23, 24].

The control diagram proposed for hysteresis control is depicted in Figure 5. The output variable of the hysteresis controller is the switching function, which represents the command to Q_2 operation, according to (5).

Hysteresis control was selected due to its robustness in managing nonlinearities and its ability to ensure stability and accuracy under varying operating conditions Unlike traditional methods such as PID control or linear quadratic regulators,

which rely on precise tuning and linearization [25], hysteresis control directly addresses the system's switching behavior by generating a binary control signal $s(t)$. This feature is critical for the CE-SA topology, where switching determines the amplifier's operational state [26, 27].

Moreover, sliding mode control (SMC), a well-established method for nonlinear systems [28], was considered. While SMC offers high robustness, its implementation introduces additional complexities, such as chattering mitigation and continuous state estimation. Hysteresis control, by contrast, is simpler to implement, computationally efficient, and naturally suited for systems with discrete switching dynamics [26, 27], as demonstrated as follows:

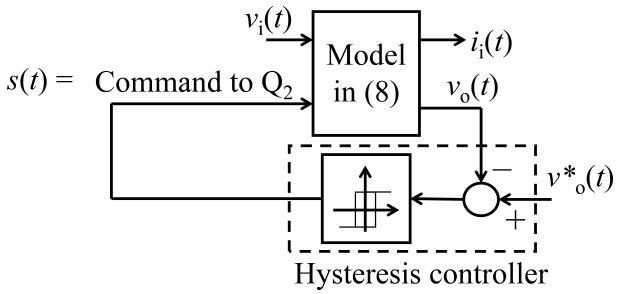

Figure 5. Proposed control diagram. Diagram of the hysteresis control, showing how the output voltage error regulates the switching state of Q_2

The hysteresis control Algorithm 1 is designed to regulate the switching state of transistor Q_2 based on the error signal $e_{vo}(t) = v_o^*(t) - v_o(t)$, where $v_o^*(t)$ is the reference output voltage, and $v_o(t)$ is the actual output voltage. The primary goal of this algorithm is to maintain the output voltage within a specified hysteresis band, ensuring accurate tracking of the reference voltage while mitigating steady-state errors.

Algorithm 1

if $v_o(t) \leq 0$ **then**
  if $e_{vo}(t) > 0.1$ **then**
    $s(t) = 0$
  else if $e_{vo}(t) < -0.1$ **then**
    $s(t) = 1$
  end if
else
  if $e_{vo}(t) > 0.1$ **then**
    $s(t) = 1$
  else if $e_{vo}(t) < -0.1$ **then**
    $s(t) = 0$
  end if
end if

The algorithm is structured into two primary cases based on the polarity of the output voltage $v_o(t)$:

- **Case 1: $v_o(t) \leq 0$ (negative half-cycle)**

  1. *Condition*: If the error signal $e_{vo}(t) > 0.1$, the switching function s(t) is set to 0.
     - *Action*: This deactivates transistor Q_2, transitioning the circuit to a configuration where R_E contributes to the system dynamics, reducing amplification.
  2. *Condition*: If $e_{vo}(t) < -0.1$, the switching function s(t) is set to 1.

- *Action*: This activates transistor Q_2, bypassing R_E, and maximizing the amplifier's gain.

- **Case 2: $v_o(t) > 0$ (positive half-cycle)**

  1. *Condition*: If $e_{vo}(t) > 0.1$, the switching function s(t) is set to 1.
     - *Action*: Transistor Q_2 is activated, bypassing R_E to maintain the desired gain.
  2. *Condition*: If $e_{vo}(t) < -0.1$, the switching function s(t) is set to 0.
     - Action: Transistor Q_2 is deactivated, introducing R_E into the circuit, and reducing the gain to maintain control.

The algorithm operates symmetrically for both positive and negative half-cycles of the output voltage. By switching Q_2 on or off depending on the error signal's deviation from the hysteresis band thresholds (±0.1), the system ensures:

- Precise tracking of the reference voltage $v_o^*(t)$.
- Rapid response to disturbances or changes in $v_o^*(t)$.
- Reduction of steady-state error during both positive and negative cycles.

This hysteresis-based control strategy is particularly effective for nonlinear systems, offering robustness against variations in system parameters and disturbances, while avoiding the need for complex linearization or dynamic compensation techniques [26, 27].

5. Simulation results

The simulation results derived from the model presented in Figure 3 and described by (8) are shown in Figure 6. These results were obtained using MATLAB-Simulink, with the specific simulation parameters provided in Table 1. The following analysis elaborates on the behavior and performance of the CE-SA system, as governed by the proposed control algorithm.

Upon system startup, the initial output voltage, $v_C(t)$, is zero, while the reference voltage, $v_C^*(t)$, is set to a peak-to-peak value of −5 V. As depicted in Figure 6a, the system demonstrates rapid convergence of $v_C(t)$ to the reference value, with minimal steady-state error, confirming the efficient initialization of the amplifier system.

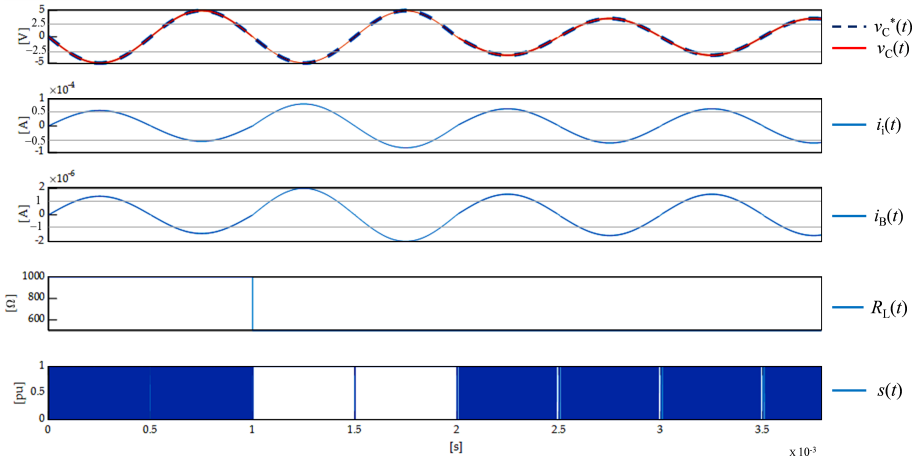

Figure 6. Simulation results. Step changes in 1 ms and 2 ms in R_L and $v_o(t)$ respectively. (**a**) Output voltage: reference $v^*_C(t)$ and measured $v_C(t)$; (**b**) Input current $i_i(t)$; (**c**) Base current $i_B(t)$; (**d**) Output resistance R_L; and (**e**) Switching function $s(t)$.

At t = 1 ms, a perturbation is introduced in the form of a step change in the load resistor R_L, which decreases from 1 kΩ to 0.5 kΩ. This perturbation induces an increase in the input current $i_i(t)$ from 0.056 mA to 0.085 mA, ensuring the stabilization of $v_C(t)$ in response to the altered load conditions, as shown in Figure 6a. The perturbation also leads to a corresponding increase in the base current $i_B(t)$, from 1.25 μA to 1.85 μA, as indicated in Figure 6c, which aligns with the relationship between the input current $i_i(t)$ and the base current $i_B(t)$.

As seen in Figure 6e, during the perturbation period (1 ms ≤ t < 2 ms), transistor Q_2 remains in the conduction state ($s(t)$ = 1), thereby placing the CE-SA in the configuration illustrated in Figure 3c, where the voltage gain A_v is at its maximum (i.e., the emitter resistor R_E is bypassed). This results in an optimal amplification mode, and as shown in Figure 7, the high-frequency ripple introduced by the hysteresis control is effectively mitigated from the output voltage $v_C(t)$.

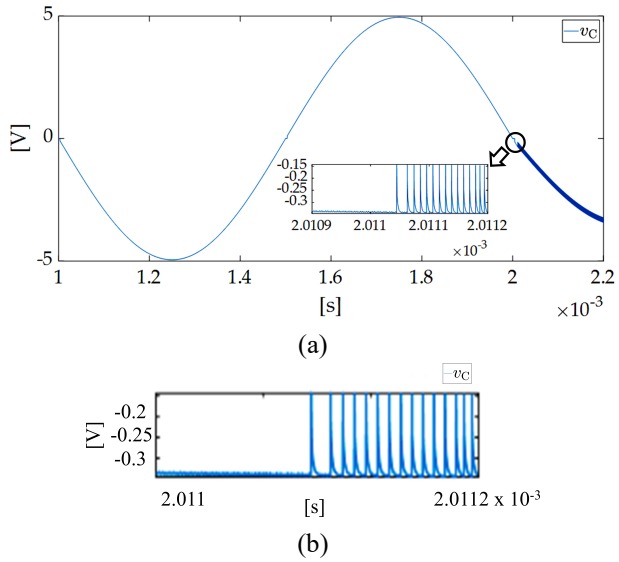

Figure 7. Zoom view of waveforms $v_o^*(t)$ and $v_o(t)$. Shows a zoomed-in view of the output voltage waveforms, demonstrating tracking accuracy and minimal steady-state error. (**a**) Waveforms $v_o^*(t)$ and $v_o(t)$. (**b**) Window view time range: 2.011 ms–2.0112 ms.

Table 1. CE-SA parameters

Parameters	Values
R_1	3 [kΩ]
R_2	15 [kΩ]
R_C	2 [kΩ]
R_E	0.5 [kΩ]
R_L	1 [kΩ]
L	1 [μH]
C	0.5 [pF]
V_{CC}	24 [V]
β	200

However, after t = 2 ms, a ripple reappears in $v_C(t)$, which is a consequence of the continuous operation of the hysteresis control loop. At t = 1.5 ms, the zero-crossing of the main variables occurs, triggering a rapid transition of the switching function $s(t)$ from 1 to 0 and back to 1, as shown in Figure 6e. This transition is indicative of the system's fast reaction to changes in the reference signal.

At t = 2 ms, a step change in the reference voltage $v_C^*(t)$ occurs, transitioning from −5 V peak-to-peak to −3.5 V peak-to-peak. As depicted in Figure 6a, the output voltage $v_C(t)$ swiftly tracks the new reference, with negligible steady-state error. The adjustments in the input current i_i(t) and base current $i_B(t)$ are illustrated in Figure 6b,c, respectively, confirming the system's stability and precise control of the output voltage.

Additionally, the behavior of transistor Q_2 confirms the correct operation of the switching function $s(t)$ through hysteresis control, as shown in Figure 6e. These results demonstrate the CE-SA's capability to adapt to changes in the operating conditions, including load perturbations and reference voltage adjustments, while maintaining accurate output tracking with minimal errors.

In conclusion, the simulation results validate the effectiveness of the proposed hysteresis control algorithm. The CE-SA system exhibits rapid response times, robust performance in the face of load changes, and precise tracking of reference voltage step changes, all while maintaining negligible steady-state errors. This confirms the suitability of the CE-SA for applications requiring flexible and dynamic voltage gain control.

6. Comparison with previous work

The proposed work introduces a CE-SA with voltage-variable gain and hysteresis control, which offers improvements in power consumption, design compactness, and control precision over previous amplifier designs. Table 2 presents a comparison between the proposed design and previous works in the field, focusing on aspects such as the amplifier type, gain control mechanisms, and system applications.

The primary innovation in this work is the integration of hysteresis control within the voltage-variable gain amplifier. Traditional systems often suffer from transient voltage fluctuations during gain transitions, particularly in sensitive applications like ultrasound imaging. By incorporating hysteresis control, this work mitigates these fluctuations, ensuring smoother operation and reducing potential artifacts in high-resolution imaging. This approach improves the overall performance of the system, making it more reliable for real-time adjustments in dynamic environments.

Another key innovation is the voltage-variable gain mechanism. While many prior works rely on discrete gain steps or interpolation techniques for gain control, the proposed amplifier offers continuous and real-time gain adjustments with finer resolution. This results in a more precise and adaptive response to varying signal conditions, which is crucial in applications like time gain compensation (TGC) in ultrasound imaging. The voltage-variable gain structure also reduces the need for additional complex control circuits, thus minimizing system complexity and enhancing system reliability.

Table 2. Comparison of the proposed CE-SA with voltage-variable gain and hysteresis control against previous work

Feature	Previous work	Proposed work
Amplifier type	Linear-in-dB VGAs, linear gain control in ultrasound imaging	CE-SA with voltage-variable gain
Gain control mechanism	Discrete TGC or continuous interpolation-based TGC	Voltage-variable gain with hysteresis control
Control scheme	Discrete or continuous feedback, interpolation-based	Hysteresis control to avoid transient voltage fluctuations
TGC functionality	Implemented through discrete gain steps or feedback-based interpolation	Real-time continuous gain control with systematic predistortion

Furthermore, the combination of real-time continuous TGC operation and voltage-variable gain provides a more efficient solution compared to traditional discrete gain-step systems. The proposed system compensates for propagation-dependent attenuation in ultrasound applications, where the signal's strength changes dynamically as it travels through various tissues. This system can accommodate varying signal conditions with minimal delay and maximum accuracy, offering significant advantages over older designs that use fixed or interpolation-based TGC.

In conclusion, while earlier works primarily focused on discrete gain control or feedback based TGC systems, the proposed amplifier offers an integrated solution that combines hysteresis control with voltage-variable gain. This design provides higher precision, reduced power consumption, and a compact form factor, making it ideal for modern ultrasound imaging systems that require real-time gain control and optimal performance.

7. Conclusions

This work presents a Common-Emitter Switched Amplifier (CE-SA) with voltage-variable gain and hysteresis control, designed to address key challenges in the field of analog amplification systems, particularly in applications such as ultrasound imaging, where dynamic signal control and precise gain regulation are paramount. The proposed amplifier introduces several innovations, including the seamless integration of hysteresis control, which mitigates transient voltage fluctuations during gain transitions, and the voltage-variable gain mechanism, which provides continuous and real-time adjustments. These advancements enhance the performance of the CE-SA, making it highly adaptable to varying signal conditions and ensuring smooth operation under fluctuating environmental parameters.

The use of hysteresis control in combination with voltage-variable gain represents a major leap forward in amplifier design. It offers a solution to the inherent nonlinearities and discrete switching behaviors typically observed in power amplifiers, providing a more robust and efficient approach to gain control. Additionally, the implementation of real-time continuous time gain compensation allows the proposed system to dynamically adjust to signal attenuation across different tissues in ultrasound imaging, improving accuracy and image resolution. These advancements lead to more reliable, compact, and power-efficient systems compared to traditional discrete gain-step or interpolation-based systems.

However, while the proposed CE-SA offers improvements in performance, there are certain limitations that must be considered. One limitation is the reliance on discrete switching states for hysteresis control, which, although effective for many applications, may not be suitable for extremely high-frequency or high-speed requirements. The current design operates effectively within the bandwidth constraints set by the voltage-variable gain mechanism, but further research may be needed to extend this bandwidth while maintaining stability and minimizing power consumption.

The practical implications of this work are vast, especially in the field of medical imaging. The proposed CE-SA has the potential to significantly enhance the quality and reliability of ultrasound systems, particularly in applications requiring fine control over the gain response. Its real-time adjustment capabilities are crucial for time-gain compensation in varying acoustic conditions, which is essential for accurate tissue characterization and imaging. Moreover, the reduced need for complex control circuits makes this amplifier well-suited for integration into miniaturized, portable medical devices, contributing to the development of more affordable and accessible diagnostic tools.

Several avenues for future research and development are envisioned based on the findings and limitations discussed in this work:

- High-frequency performance: While the current design offers excellent performance within a defined bandwidth, future work could investigate the extension of the amplifier's bandwidth to accommodate high-frequency applications, such as in wireless communication systems or advanced radar technologies. This could involve optimizing the hysteresis control to manage switching transients at higher frequencies.
- Advanced power efficiency: Given the increasing demand for low-power, energy-efficient devices, further advancements in power optimization techniques could be explored. Techniques such as adaptive biasing, low-power active components, or even energy harvesting methods could be integrated to further reduce the power consumption of the amplifier without compromising performance.
- Integration with digital systems: The hybrid approach of combining analog control via hysteresis with digital signal processing (DSP) systems offers opportunities for more complex control strategies. Future work could focus on integrating the CE-SA design with digital systems for adaptive gain control based on real-time signal analysis, creating a more intelligent and responsive amplifier system.
- Miniaturization for portable devices: The compactness of the proposed CE-SA makes it suitable for portable ultrasound imaging systems. However, additional efforts are required to optimize the size and weight further, particularly in terms of miniaturizing passive components like resistors, capacitors, and inductors without sacrificing performance. This would enable the development of portable, battery-operated devices suitable for use in remote or resource-limited settings.

- Nonlinear compensation techniques: To enhance the robustness of the system under extreme conditions, the incorporation of advanced nonlinear compensation techniques, such as pre-distortion or dynamic control schemes, could further improve the performance of the CE-SA. These approaches could be particularly useful in applications with large dynamic range requirements, where traditional linear compensation methods may fail.
- Testing and validation in clinical settings: While the theoretical design and simulations suggest promising results, practical testing in real clinical environments is essential to validate the system's performance. This would include assessing the CE-SA in dynamic, high-resolution imaging scenarios, ensuring that it meets the stringent accuracy, reliability, and safety requirements for medical devices.

In summary, the CE-SA with voltage-variable gain and hysteresis control presented in this work attempts to offer an advancement in amplifier technology, providing enhanced precision, power efficiency, and reliability for applications in ultrasound imaging and other dynamic signal processing environments. While the system exhibits good performance within the current design parameters, further research aimed at extending its capabilities, optimizing its power consumption, and integrating it with emerging technologies could unlock even greater potential for future practical applications. The integration of hysteresis control and real-time TGC represents an innovative approach that addresses the critical challenges of gain regulation and signal fidelity.

Conflict of interest

The authors declare no conflict of interest.

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