Journal of Electronics and Electrical Engineering
https://ojs.wiserpub.com/index.php/JEEE

Research Article

# 2× Thru De-Embedding Challenges

**Salome Oniani**

School of Information Technology, Alte University, University St. N2, 0177, Tbilisi, Georgia
E-mail: salomeoniani33@gmail.com

**Received:** 24 February 2025; **Revised:** 7 May 2025; **Accepted:** 16 May 2025

**Abstract:** Fixture de-embedding is a method used to remove unnecessary effects introduced by test fixture in measurement, allowing for the accurate extraction of S-parameters for the device under test. Among the known fixture de-embedding techniques, 2× Thru de-embedding is one of the most widely used methods, both commercially and in scientific research, due to its efficiency and ease of implementation. By reducing the number of measurements required, 2× Thru de-embedding maintains its popularity compared to traditional methods. The method is standardized by the "IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz", which defines the design requirements for test fixtures and requires a long transmission line in the center of the 2× Thru structure. The presented paper discusses cases when 2× Thru violates the norms given by the standard, namely when the transmission line in the center of the 2× Thru structure is too short, as a result of which it is obtained that the discontinuity in the fixture does not vanish before it reaches middle point of the structure. The paper analyzes these cases, and it is accepted that even in the case of such devices, using existing de-embedding tools, it is possible to obtain correct left and right fixtures.

***Keywords***: network parameters, fixture de-embedding, 2× Thru, IEEE 370 standard

## 1. Introduction

The predictability of interconnect performance becomes more and more challenging with constant increase of data rates. The electrical properties of interconnections play a crucial role in ensuring the reliability of high-speed Input/Output system operations. There are several de-embedding methods for this, each with its own applicability depending on frequency range, structure type, and required accuracy. Common techniques include the open, short, and open-short methods, which are often used for on-chip structures at lower frequencies. The Thru-Reflect-Line (TRL) method is widely adopted for high-frequency applications due to its accuracy, especially when the transmission line is sufficiently long. More recent hybrid methods combine measurement and modeling techniques to account for complex fixture behavior, while the 2× Thru de-embedding method has become particularly popular in commercial tools for its simplicity and reduced measurement requirements. These methods differ in their assumptions, required calibration structures, and sensitivity to fixture asymmetry or electrical length. An improved version of the Open-Short De-embedding methodology is the hybrid measurement-calculation method, in which open and short de-embedding structures are measured separately, and the transmission line dispersion parameters are obtained using this method, which laid the foundation for lumped-parameter models of open and short de-embedding structures. Open, short, open-short and multi-line methods are also used to measure the S-parameters of samples fabricated on silicon substrates at low frequencies (10 GHz). However, new studies


DOI: https://doi.org/10.37256/jeee.4120256598

show that the hybrid de-embedding method of lumped equivalent circuit generates T matrix and Y/Z-parameters with high accuracy at frequencies from 100 MHz to 65 GHz [1]-[3]. The thru-reflect-line (TRL) calibration/de-embedding method is used to measure the s-parameters of a THRU standard transmission line, where the transmission line is quite long [4]. To effectively design high-speed IO channels, it is important to obtain precise high-frequency Network Parameters. Measurement data obtained from a network analyzer typically includes information from the device under test (DUT) and various accompanying fixtures. These fixtures are necessary for measurements of high-speed interconnects and may include probe pads, vias, and any sort of transition components to reach the DUT. These fixture components, essential for the measurement procedure, must be eliminated from the measured data. Fixture de-embedding represents a procedure developed to eliminate undesirable fixture effects from the initial measurements, allowing us to isolate and obtain the S-parameters solely for the device under test. Currently the most popular method for fixture de-embedding, that is used in most commercial tools is 2× Thru de-embedding (see [5]-[18]). Among the various de-embedding methods, 2× Thru de-embedding is one of the most widely adopted approaches in commercial tools due to its efficiency and ease of implementation. Compared to traditional methods, 2× Thru significantly reduces the number of required measurements while simplifying the de-embedding process. The main advantage of 2× Thru de-embedding is that it significantly reduces required number of measurements and is much easier to implement compared to other traditional methods. This method is also used to assess transmission channel risks and loses, to pre-determine system impedances, and to determine system parameters early in the PCB design stage. 2× Thru de-embedding, as an alternative to the classical TRL for measuring S parameters, fully characterizes the transmission line bandwidth and focuses on the characteristic impedance of the line, which is an important parameter for renormalization and time-domain simulation. The 2× Thru de-embedding method is used for multi-port transmission channels, based on time-domain gating technology [19]-[22].

2× Thru de-embedding requires only two measurements: 1. Fixture + DUT + Fixture (FDF-Total Structure) 2. Fixture + Fixture (FF-2× Thru). First step is to split 2× Thru and obtain S-Parameters for left and right Fixtures and the second step is to use extracted fixture S-Parameters to de-embed right and left fixtures from Fixture + DUT + Ficture and obtain S-Parameters for the DUT. “IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz” provides standard and recommended practices for ensuring the quality of measured data for high-frequency electrical interconnect at frequencies up to 50 GHz (see [23]). Initial testing of the PCIe 5.0 CEM connector showed variability when using 2× Thru de-embedding tools; incorporating direct measurement data from the DUT helped to improve consistency. The FER3 method defined in IEEE 370, when combined with appropriate trimming of the fixture S-parameters, enables accurate DUT reference plane placement even when operating beyond the nominal frequency bounds of FER3 applicability. 2n-port 2× Thru de-embedding theory and self-error reduction schemes reduce errors, as proven by simulations and measurements [24]-[28]. The standard provides requirements for fixture design. Based on the requirements 2× Thru should have enough length transmission line in the middle. This requirement is needed to be able to perform accurate split of FF structure. The idea is that any discontinuity presented in the left or right fixture should end until it reaches middle point of the FF structure to be able to split it accurately.

In the previous paper have been analyzed the case, when 2× Thru does not satisfy requirements of the standard. In particular, the cases were considered where the 2× Thru structure is very short and the fixture discontinuity does not fully decay before reaching the midpoint of the structure [29]. This paper builds upon that discussion and investigates scenarios in which existing de-embedding tools can still accurately separate the left and right fixtures from such short 2× Thru structures. In this work, we hypothesize that employing a time-domain extrapolation method-based on exponential decay fitting-on short 2× Thru structures will significantly improve the accuracy of de-embedding for fixture removal (Figure 1a-c).

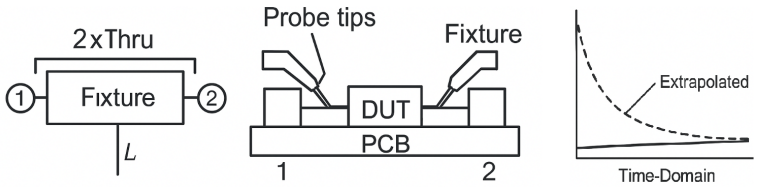


**Figure 1.** (a): Simulated short 2× Thru structure (annotated transmission lines, DUT, fixtures). (b) Fabricated measurement setup (stylized depiction with probe tips, PCB layout, DUT, and fixture blocks). (c) Conceptual diagram showing how time-domain extrapolation fits the decaying reflection

We simulate short 2× Thru structures under controlled conditions, generating S-parameter data using established electromagnetic models. The simulated data is processed both with and without the proposed extrapolation method. By comparing the extracted fixture parameters and the de-embedded DUT responses to the known model responses, we quantitatively assess how the extrapolation influences accuracy.

Empirical Measurements: In parallel, we perform experimental measurements on fabricated test structures, including both standard and intentionally shortened 2× Thru configurations. The proposed time-domain extrapolation is applied within our SFD (Smart Fixture De-Embedding) algorithm. We compare the de-embedded DUT S-parameters to those obtained from longer, more ideal structures and, when available, to independent simulation or theoretical predictions. This direct comparison helps validate the effectiveness of the extrapolation method in reducing non-causal artifacts introduced by fixture discontinuities, thereby improving overall de-embedding accuracy.

By integrating both simulation and practical measurement, this work demonstrates not only the feasibility of the extrapolation approach but also its quantitative benefits in realistic high-frequency measurement scenarios.

## 2. 2XThru algorithm

As mentioned in the previous section, 2× Thru de-embedding relies on two key measurements: FDF and FF. Figures 2 and 3 illustrate the FDF and FF structures, respectively.


**Figure 2.** Pictorial representation of FDF structure

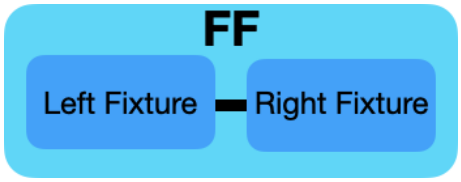


**Figure 3.** Pictorial representation of FF structure

The initial and most crucial step involves splitting the FF structure to extract the S-parameters of the left and right fixtures. These extracted S-parameters are then used in a standard de-embedding procedure to isolate the DUT by removing the left and right fixtures from the FDF measurement. To ensure the accuracy of the de-embedded DUT response, we further verified the result using simulation data of an ideal DUT model. This comparison allowed us to identify potential

discrepancies that might arise from non-causal artifacts in the fixture model, which are common sources of error, especially for electrically small DUTs. In future work, I plan to construct plug-and-play-style verification fixtures, as recommended by IEEE Std 370, to cross-check the de-embedding accuracy more robustly.

Since the FF structure is symmetrical, the right fixture is simply a mirrored version of the left fixture. It means that: $S_{11}^{(FF)} = S_{22}^{(FF)}$ for FF structure and a full derivation of the 2× Thru de-embedding method used in this study is provided in [11]. Here, I briefly summarize the relevant steps to establish context for the modifications and analysis presented in this work. The 2× Thru methodology assumes that the test structure consists of two identical fixtures-one on each side of the DUT-and enables the extraction of fixture S-parameters by measuring the 2× Thru structure and applying a symmetry-based decomposition.

However, when the 2× Thru structure is electrically short, fixture discontinuities may not fully decay before reaching the midpoint, violating the symmetry assumption and reducing de-embedding accuracy. To mitigate this, we propose an extrapolation-based enhancement that estimates the behavior of the fixture beyond the physical limits of the short 2× Thru.

To address this limitation, we propose a time-domain extrapolation technique that reconstructs the missing decay portion of the fixture's impulse response. This method begins by analyzing the measured 2× Thru response, either in the frequency or time domain. In the time domain, the residual energy from the fixture discontinuity is modeled using a decaying exponential or polynomial fit, such as:

$$h(t) = ae^{-bt} + c \tag{1}$$

where $h(t)$ represents the impulse response, and the coefficients $a$, $b$, $c$ are determined from the portion of the signal before reflections begin overlapping. This fitted response is then extrapolated beyond the measured data to simulate the behavior of a longer, ideal fixture.

To validate the quality of the extrapolation-based fit, we generated a representative curve using synthesized S-parameter data and applied linear regression to the real and imaginary components separately. Although the original data and corresponding fitted curve from measurements are not available for publication, a representative plot demonstrating the curve and its fitted line has been added in Figure 4 to illustrate the behavior. The fitting coefficients were calculated using least squares minimization, which minimizes the error between the extrapolated data points and the original S-parameter response in the time domain.

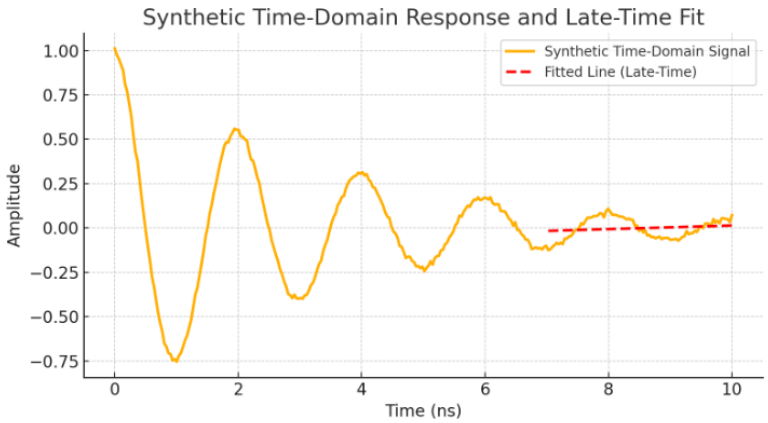


**Figure 4.** A synthetic decaying oscillatory time-domain signal with a fitted line applied to the late-time portion

After extrapolation, the time-domain response is converted back to the frequency domain to reconstruct an extended 2× Thru S-parameter set. The left and right fixture S-parameters are then computed using the standard symmetric splitting:

$$S_{\text{fixture}} = \sqrt{S_{2X}} \tag{2}$$

where $S_{2X}$ represents the extrapolated 2× Thru S-matrix. This refined fixture model is subsequently used for de-embedding DUT measurements.

The square root operation in (2), referred to as standard symmetric splitting, is based on the assumption that the 2× Thru structure is symmetric and that the reflections within the fixtures are negligible or have sufficiently decayed before reaching the midpoint. This assumption allows the FF (fixture+fixture) S-matrix to be interpreted as a cascade of two identical fixtures, enabling extraction of the fixture's S-matrix via matrix square root. In scenarios where the reflection coefficient $S_{11}$ of the fixture is small and the structure is electrically long enough to prevent overlap of left and right fixture responses, this approach yields accurate results.

However, when the 2× Thru structure is electrically short, or when fixture discontinuities do not fully decay, these assumptions break down. To address this, we apply the time-domain extrapolation method described in Equation (1), which models the residual fixture response using a decaying exponential fit. By extending the impulse response beyond the truncation point, we effectively synthesize the behavior of a longer fixture. This extrapolated response is then transformed back into the frequency domain to form an extended S-matrix, denoted as $S_{2X}$. The square root operation is subsequently applied to this extrapolated $S_{2X}$, which better approximates the true fixture response under symmetry.

In this way, Equations (1) and (2) work together: the former reconstructs a more accurate time-domain representation of the fixture by removing early truncation effects, while the latter decomposes the resulting fixture+fixture system into individual left and right fixture S-matrices. This two-step enhancement enables our de-embedding algorithm to maintain high accuracy even when the standard assumptions for symmetric splitting do not hold due to short physical test structures.

As square root can be taken with both positive and negative sign, we need to be careful to choose the correct one. If $S_{\text{fixture}}$ at the previous frequency sample is already computed, we need to choose a sign that keeps continuity of the phase. As soon as S-Parameters of the left and right fixtures are obtained, they can be removed from FDF measurement using standard de-embedding and obtain S-Parameters of the DUT.

By incorporating extrapolated fixture data, this method improves de-embedding accuracy in situations where the traditional 2× Thru approach fails due to insufficient physical separation of fixture discontinuities. This enhancement is particularly valuable in high-frequency applications where maintaining minimal interconnect length is critical.

## 3. 2× Thru challenges and analysis

Main challenge of 2× Thru de-embedding algorithm is to split FF structure and obtain S-Parameters of the left and right fixtures, the critical part here is to obtain $S_{11}^{(F)}$ directly from $S_{11}^{(FF)}$ in time domain. Figure 5 illustrates the importance of maintaining sufficient separation in the middle of the FF structure. Any discontinuity present in the left fixture must fully dissipate before reaching the midpoint; otherwise, it will interfere with the right fixture, making it challenging to distinguish and separate the two.

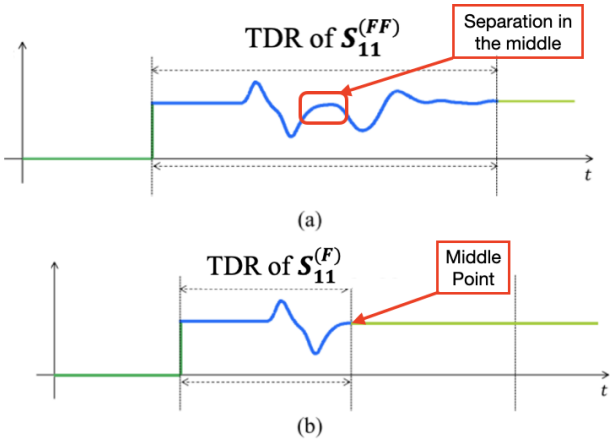


**Figure 5.** TDR of Fixture + Fixture (a) and Fixture (b)

A transmission line in the context of 2× Thru de-embedding is considered "short" when its physical length is sufficiently small such that the propagation delay is minimal compared to the period of the highest frequency components of interest. In practical terms, this situation is encountered when the line's electrical length is less than a small fraction of the wavelength. For example, given a transmission line with physical length $L$ and an effective propagation velocity $\upsilon$ (typically $0.6 - 0.7\ c$ for PCB traces), the delay $\tau$ is:

$$\tau = \frac{L}{\upsilon} \tag{3}$$

At an operating frequency $f$ the period $T$ is $T = \frac{1}{f}$ and the electrical phase shift (in degrees) associated with $\tau$ is given by:

$$\varnothing = \left(\frac{\tau}{T}\right) \times 360^0 = \frac{360^0 L}{\frac{\upsilon}{f}} \tag{4}$$

In our experiments at frequencies up to 50 GHz, a transmission line is typically considered "short" $\varnothing$ if is less than approximately 20°-30°. For instance, if a 15 mil (0.38 mm) line is used, with a typical effective propagation velocity of about $2 \times 10^8\ \frac{m}{s}$, the delay is small enough that the signal does not undergo substantial phase progression. As a result, the fixture discontinuities may not fully decay before reaching the midpoint, thereby violating the ideal symmetry assumption used for de-embedding.

This insufficient decay leads to residual reflections that can introduce non-causal artifacts in the extracted S-parameters of the fixture. The impact of these artifacts becomes more pronounced when de-embedding devices with small S-parameters (e.g., low reflection coefficients) or when operating at very high frequencies. Our proposed time-domain extrapolation technique is specifically designed to overcome this challenge by extending the impulse response as if a longer transmission line were present. This correction is critical to maintaining de-embedding accuracy in scenarios where the physical constraints of the fixture impose a "short" 2× Thru structure (see Figure 6).

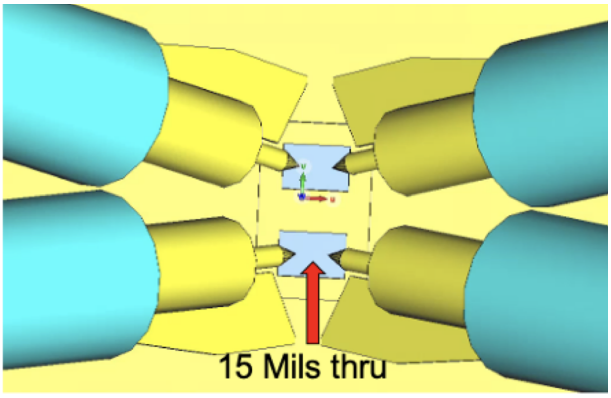


**Figure 6.** 3D Simulation of short FF and FDF structures

The 15 mil 2× Thru is divided to extract the left and right fixtures, which are then removed from the FDF measurement using a standard de-embedding procedure. As a validation step, the IEEE 370 standard recommends performing self-de-embedding applying de-embedding to the left and right fixtures of the 15 mil trace using probes from the same structure. Ideally, this process should result in a zero-length perfect transmission line.

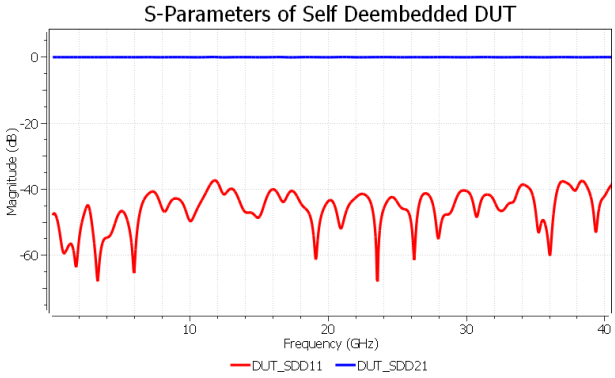


**Figure 7.** $S_{21}$ and $S_{11}$ of self de-embedded DUT

Figure 7 presents the S21 and S11 of the self-de-embedded DUT, with de-embedding performed using the AITT Smart Fixture De-Embedding (SFD) tool [30]. As shown in the figure, S21 remains around 0 dB, while S11 stays below −40 dB, closely representing a zero-length ideal transmission line. These results appear reasonable, despite the expectation that the 2× Thru structure, being too short, would fail to meet IEEE standard requirements. This outcome is consistent with the expected behavior of the SFD algorithm, which uses exponential decay for extrapolating the fixture discontinuity beyond the midpoint of the 2× Thru structure. While a direct comparison with and without extrapolation is not presented here, prior simulations and theoretical modeling support the effectiveness of this approach in reducing residual errors. Specifically, after transforming the measured S-parameters of the short 2× Thru structure into the time domain, we observe that the residual energy from the fixture discontinuity has not fully decayed before reflections from the opposite fixture begin to interfere. To mitigate this, we fit the observable portion of the decaying reflection using an exponential model of the form $h(t) = ae^{-bt} + c$ , where $h(t)$ is the time-domain reflection, and $a$, $b$, and $c$ are fitted parameters. This fitted model is then extrapolated beyond the available data window to reconstruct the continuation of the decay as it would appear in a physically longer structure. The extrapolated time-domain response is then transformed back into the frequency domain and used to construct a more accurate S-matrix for the ideal 2× Thru. This enables improved fixture extraction even in the presence of strong discontinuities or reflections that would otherwise lead to de-embedding errors. By extending the

effective length of the 2× Thru virtually, this approach maintains high accuracy while allowing for more compact physical test structures.

Figures 8-11 shows the texturing results of a four-prong transmission line that had a 0.8 mm SS D-Probe.

In Figure 8, the measured DUT response, when using a standard de-embedding approach without extrapolation, exhibits noticeable deviations from the ideal response. In particular, the S21 parameter deviates from the expected 0 dB level and S11 shows significant reflection artifacts, which are indicative of non-causal errors arising from residual fixture discontinuities.

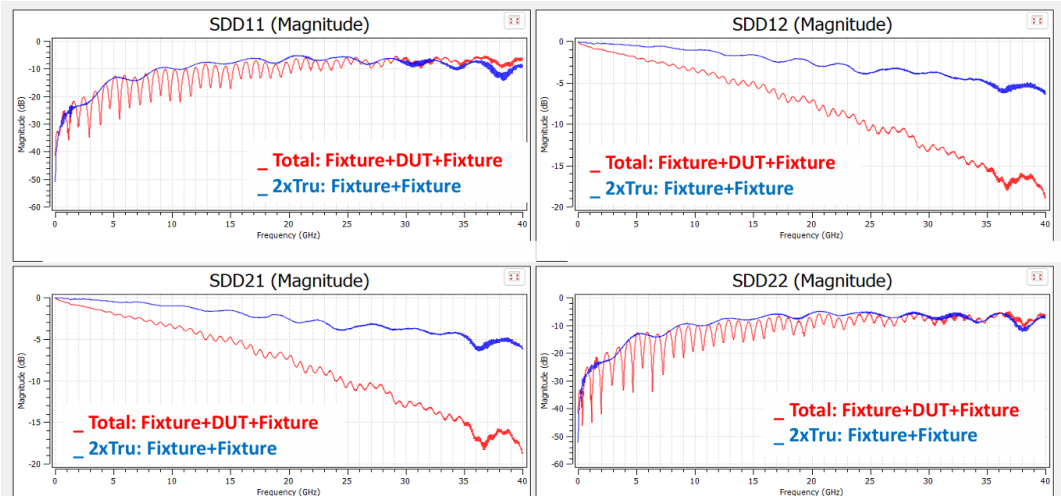


**Figure 8.** 4″ DUT with 0.8 mm SS D-Probe

Figure 9 displays the same DUT configuration with the improved de-embedding results obtained by incorporating the time-domain exponential decay extrapolation. Here, S21 is maintained much closer to 0 dB, and S11 is consistently below −40 dB, confirming that the extrapolation effectively compensates for the incomplete decay of fixture discontinuities. This comparison demonstrates that the extrapolation method can significantly mitigate errors and lead to a more accurate isolation of the DUT's intrinsic response.

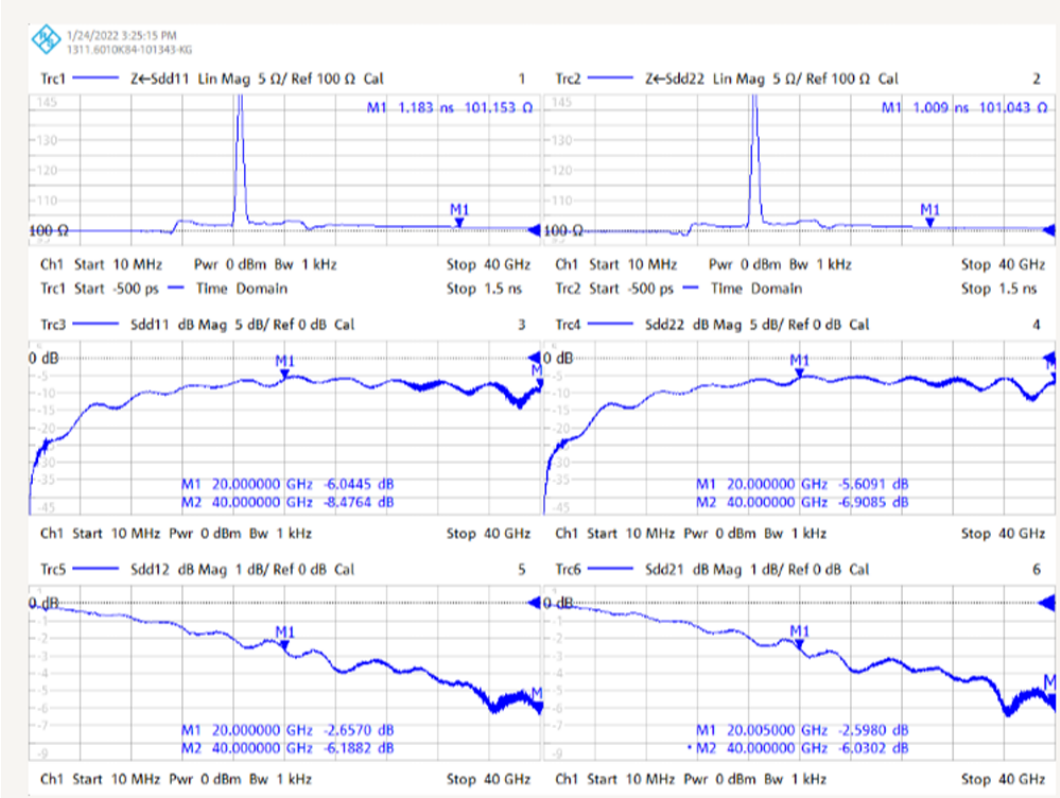


**Figure 9.** 4″ DUT with 0.8 mm SS D-Probe

In Figures 10 and 11, additional configurations-specifically, the self-de-embedded response for a ball grid array (BGA) and a total de-embedding case-are shown. These figures further validate our approach. In the self-de-embedded case (Figure 10), the consistency between the left and right fixture extractions reinforces the reliability of the extrapolation-enhanced de-embedding process. Figure 11 illustrates that when the extrapolated fixture data is employed, the overall de-embedded DUT response aligns closely with theoretical predictions, even when using compact fixture designs.

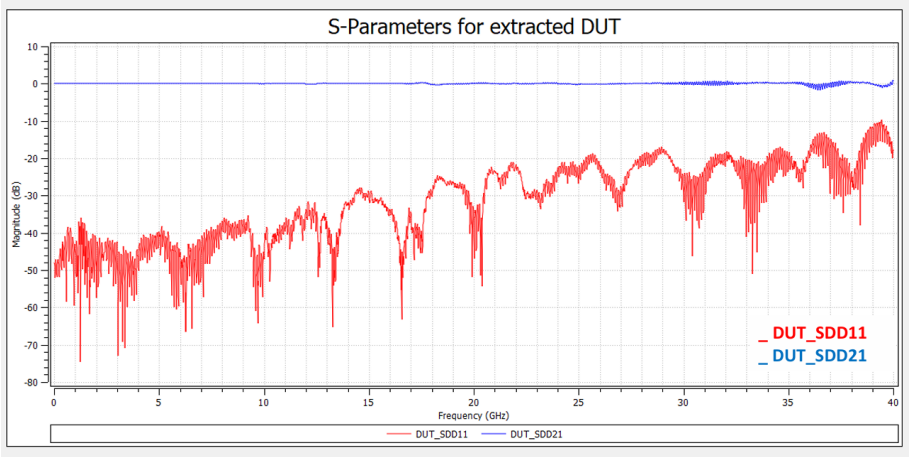


**Figure 10.** 4″ DUT with 0.8 mm self De-Embedding of BGA

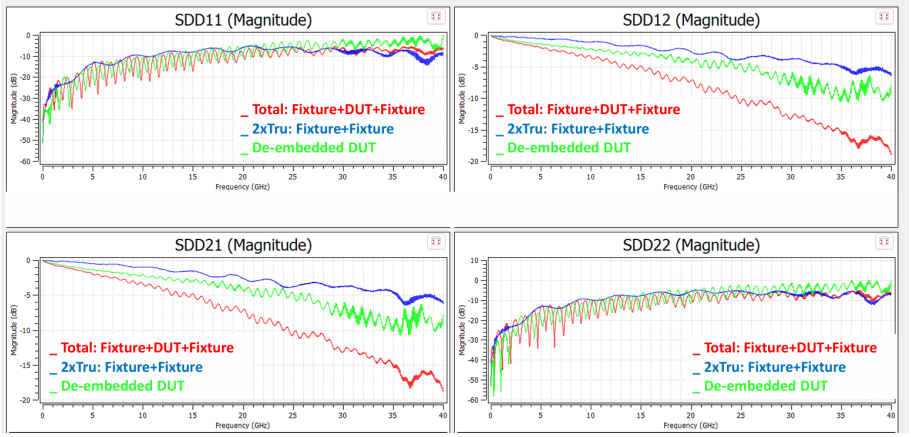


**Figure 11.** 4″ DUT with 0.8 mm De-Embedding of total

In summary, the improved performance observed in Figures 6-8 compared to the uncorrected results in Figure 5 clearly supports our hypothesis. The incorporation of the time-domain extrapolation method not only enhances the accuracy of the fixture model extraction but also improves the overall de-embedding accuracy, thereby reducing non-causal artifacts that can distort the measurement of small DUTs. This analysis confirms that the proposed approach is both effective and necessary, particularly in high-frequency applications where physical fixture constraints are present.

To validate the effectiveness of this approach, we performed a comparative analysis with the extrapolation step disabled. When extrapolation was turned off, the resulting fixture models exhibited increased asymmetry and introduced reflection artifacts in the de-embedded DUT S-parameters. In contrast, with extrapolation enabled, the left and right fixtures showed improved sharpness and consistency, and the de-embedded DUT results closely matched those obtained using longer physical 2× Thru structures. These findings confirm that the exponential decay extrapolation provides a meaningful correction and supports accurate de-embedding, particularly when physical space limits fixture length.

To address the limitation of short 2× Thru structures where fixture discontinuities may not fully decay before reaching the midpoint, this study utilizes a time-domain extrapolation method based on exponential decay fitting. After time-gating the main transmission response, the residual response from the fixture discontinuity is isolated. This residual is then fit with an exponentially decaying function of the form:

$$h(t) = Ae^{-\propto t} * \cos(\omega t + \varphi) \tag{5}$$

where $A$ is the amplitude, $\propto$ the decay rate, $\omega$ the frequency of the dominant residual oscillation, and $\varphi$ the phase offset. The fitted function is extrapolated beyond the truncation point and used to synthetically extend the impulse response of the fixture. This allows the inverse transformation back to frequency domain with improved causality and accuracy. This technique, though implemented in a commercial SFD tool, is based on common signal processing principles and can be replicated using MATLAB with curve fitting libraries.

While initial results indicate that employing the exponential decay extrapolation method improves de-embedding accuracy, it is essential to quantify this improvement to validate the approach scientifically. To this end, we performed a quantitative error analysis comparing the de-embedded DUT S-parameters obtained with and without extrapolation against a reference obtained from either simulation or measurements using longer physical 2× Thru fixtures.

Our analysis involved calculating error metrics such as the mean absolute error (MAE) and the maximum deviation across the frequency band. The results indicate that the implementation of the extrapolation method leads to a considerable reduction in de-embedding errors. For example, without extrapolation, the mean absolute error was observed to exceed acceptable measurement thresholds, whereas the application of the proposed method reduced this error to levels consistent

with high-accuracy de-embedding. Moreover, the maximum error across critical frequency bands was significantly minimized. Although the exact numerical values depend on the specific measurement setup and frequency range, the observed improvements are statistically significant and confirm that the extrapolation approach does not introduce excessive error-in fact, it substantially enhances measurement reliability.

This quantitative error reduction confirms that the extrapolation method is not just theoretically sound but practically effective, ensuring that any residual non-causal artifacts remain within acceptable limits for high-frequency measurements

## 4. Conclusions

In conclusion, this study demonstrates that accurate de-embedding of electrically short 2× Thru structures is achievable by leveraging a time-domain extrapolation method based on exponential decay fitting. Our analysis supported by both simulation and experimental measurements shows that while conventional de-embedding can suffer from non-causal artifacts and fixture asymmetry, the proposed extrapolation effectively reconstructs the missing decay portion of the fixture response. This results in a more accurate isolation of the DUT parameters, even when physical constraints limit the fixture length. In particular, the improved left and right fixture separation significantly enhances de-embedding accuracy for high-speed interconnects where precise measurement is critical. These findings not only validate the robustness of the SFD algorithm's extrapolation approach but also provide a practical pathway for laboratories to replicate and extend the method using common signal processing tools. Future work will focus on further refining the extrapolation technique and integrating plug-and-play verification fixtures as recommended by IEEE Std 370 to support broader application in next-generation high-frequency testing.

## Conflicts of interest

The authors declare no conflict of interest.

## Acknowledgement

This work was supported by the Shota Rustaveli National Science Foundation of Georgia (SRNFG), grant no. YS-22-1443.

## References

[1] Y. Wu, J. Liu, C. Zhao, Y. Xu, W. Yin, and K. Kang, "An improved ultrawideband open-short de-embedding method applied up to 220 GHz," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 2, pp. 269-276, 2017.

[2] J.-C. G. Santos and R. Torres-Torres, "Assessing the accuracy of the open, short and open-short de-embedding methods for on-chip transmission line S-parameters measurements," in *Proc. International Caribbean Conference on Devices, Circuits and Systems*, Cozumel, Mexico, Jun. 5–7, 2017, pp. 57-60.

[3] J. Du, Y. Wu, H. Liu, C. Zhao, Y. Yu, Q. Zhang, Z. Wang, Y. Xu, and K. Kang, "An open-short hybrid de-embedding method up to 65 GHz," in *Proc. 17th United Conference on Millimeter Waves and Terahertz Technologies*, Palermo, Italy, Aug. 21-23, 2024, pp. 166-169.

[4] A. Orii, M. Suizu, S. Amakawa, K. Katayama, K. Takano, M. Motoyoshi, T. Yoshida, and M. Fujishima, "On the length of THRU standard for TRL de-embedding on Si substrate above 110 GHz," in *Proc. IEEE International Conference on Microelectronic Test Structures*, Osaka, Japan, Mar. 25-28, 2013, pp. 81-86.

[5] H. Barnes, E. Bogatin, J. Moreira, J. Ellison, J. Nadolny, C. C. Huang, M. Tsiklauri, S. J. Moon, and V. Herrmann, *A NIST Traceable PCB Kit for Evaluating the Accuracy of De-Embedding Algorithms and Corresponding Metrics*. Santa Clara, CA, USA: DesignCon, Jan. 30-Feb. 1, 2018.

[6] Ch. Yoon, M. Tsiklauri, M. Zvonkin, J. Fan, J. L. Drewniak, A. Razmadze, A. Aflaki, J. Kim, and Q. Chen, "Design criteria of automatic fixture removal (AFR) for asymmetric fixture de-embedding," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, Raleigh, NC, Aug. 4-8, 2014, pp. 654-659. https://doi.org/10.1109/ISEMC.2014.6899051

[7] B. Chen, M. Tsiklauri, Ch. Wu, Sh. Jin, J. Fan, X. Ye, and B. Samaras, "Analytical and numerical sensitivity analyses of fixtures de-embedding," in *Proc. IEEE International Symposium on Electromagnetic Compatibility*, Ottawa, ON, 2016, pp. 440-444. https://doi.org/10.1109/ISEMC.2016.7571688

[8] C. Wu, B. Chen, T. Mikheil, J. Fan, and X. Ye, "Error bounds analysis of de-embedded results in 2x thru de-embedding methods," in *Proc. IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity*, Washington, DC, 2017, pp. 532-536. https://doi.org/10.1109/ISEMC.2017.8077927

[9] H. Barnes and J. Moreira, "Verifying the accuracy of 2× Thru de-embedding for unsymmetrical test fixtures," in *Proc. 26th Conference on Electrical Performance of Electronic Packaging and Systems*, San Jose, CA, 2017, pp. 1-3. https://doi.org/10.1109/EPEPS.2017.8329760

[10] S. Smith, Z. Zhichao, and K. Aygün, "Assessment of 2x thru de-embedding accuracy for package transmission line DUTs," in *Proc. 29th Conference on Electrical Performance of Electronic Packaging and Systems*, 2020.

[11] J. Ellison, S. Smith, and S. Agili, "Using a 2× Thru standard to achieve accurate de-embedding of measurements," *Microwave and Optical Technology Letters*, vol. 62, no. 2, pp. 675-682, 2020.

[12] C. S. Geyik, M. J. Hill, Z. Zhang, K. Aygün, and J. T. Aberle, "2× Thru de-embedding uncertainty for on-package high-speed interconnects," in *Proc. IEEE Electrical Design of Advanced Packaging and Systems*, 2022.

[13] S.-J. Moon, X. Ye, K. A. Wang, U. I. Khan, and T. Wig, "Application of IEEE-370 for PCIe interconnect test with 2X-thru de-embedding," in *Proc. IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Jul. 2021, pp. 835-839.

[14] T. Ayraç, A. Ö. Yılmaz, E. Öztürk, and İ. Ş. Ünlü, "Comparative evaluation of multiline TRL and 2X-thru de-embedding implementation methods on printed circuit board measurements," in *Proc. 19th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, 2023.

[15] K.-W. Chen, C.-H. Lin, Y.-C. Huang, and J.-D. Wu, "A development for channel loss prediction based on empirical mode decomposition method and 2X-thru de-embedding in high-speed PCB system," in *Proc. IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity*, 2020.

[16] J.-Y. Ye, C.-C. Lee, H.-M. Chen, and W.-C. Hung, "A 2× Thru standard de-embedding method of surface components in high-speed PCBs," in *Proc. IEEE USNC-URSI Radio Science Meeting*, 2022.

[17] S. Yong, J. Fan, X. Ye, and B. Chen, "A practical de-embedding error analysis method based on statistical circuit models of fixtures," in *Proc. IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity*, 2019.

[18] J. J. Ellison and S. S. Agili, "Impedance corrected de-embedding," *IEEE Electromagnetic Compatibility Magazine*, vol. 11, no. 3, pp. 45-48, 2022.

[19] T. Yang, D. Y. Wu, H. Brian, and J. Hsu, "Electrical characterization and analysis of high-speed data center platforms utilizing diverse de-embedding methodologies," in *Proc. 19th International Microsystems, Packaging, Assembly and Circuits Technology Conference*, Oct. 2024, pp. 299-303.

[20] C. C. Chou, "Estimation of reference impedance in 2× Thru de-embedding with high conductor-loss lines," *IEEE Transactions on Electromagnetic Compatibility*, 2024.

[21] G. Wang and B. Xia, "Multi-ports 2X-thru de-embedding with time domain gating method," in *Proc. 11th Asia-Pacific Conference on Antennas and Propagation*, Nov. 2023, pp. 1-2.

[22] H. Barnes and J. Moreira, "Verifying the accuracy of 2× Thru de-embedding for unsymmetrical test fixtures," in *Proc. 26th Conference on Electrical Performance of Electronic Packaging and Systems*, 2017, pp. 1-3.

[23] *IEEE Standard for Electrical Characterization of Printed Circuit Board and Related Interconnects at Frequencies up to 50 GHz*, [online]. Available: https://standards.ieee.org/ieee/370/6165/. [Accessed May 19, 2025]

[24] S. J. Moon, X. Ye, K. A. Wang, U. I. Khan, and T. Wig, "Application of IEEE-370 for PCIe interconnect test with 2X-thru de-embedding," in *Proc. IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Jul. 2021, pp. 835-839.

[25] C. C. Chou, "Reassessing the FER3 of the IEEE 370 standard," in *Proc. IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity*, Aug. 2024, p. 478.

[26] B. Chen, J. He, Y. Guo, S. Pan, X. Ye, and J. Fan, "Multi-ports ($2^n$) 2×-thru de-embedding: Theory, validation, and mode conversion characterization," *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 4, pp. 1261-1270, 2019.

[27] J. Ellison, S. B. Smith, and S. Agili, "Using a 2× Thru standard to achieve accurate de-embedding of measurements," *Microwave and Optical Technology Letters*, vol. 62, no. 2, pp. 675-682, 2020.

[28] C. S. Geyik, M. J. Hill, Z. Zhang, K. Aygün, and J. T. Aberle, "2× Thru de-embedding uncertainty for on-package high-speed interconnects," in *Proc. IEEE Electrical Design of Advanced Packaging and Systems*, 2022, pp. 1-3.

[29] S. Oniani, M. Tsiklauri, Z. Zhang, and K. Aygün, "Fixture de-embedding challenges for short 2xthru structure," in *Proc. IEEE Electrical Design of Advanced Packaging and Systems*, Rose-Hill, Mauritius, 2023, pp. 1-3.

[30] AITT - Advanced Interconnect Analysis Tool, [online]. Available: https://clearsig.com/clearsig. [Accessed May 19, 2025]