Journal of Electronics and Electrical Engineering
https://ojs.wiserpub.com/index.php/JEEE

Research Article

Particle Swarm Optimization for Fuzzy Adaptive Sliding Mode Control in Half-Bridge Buck Converter: A Comparative Analysis

Salah Eltief*, M. Matin

Daniel Felix Ritchie School of Engineering and Computer Science, University of Denver, 2155 E. Wesley Ave., Denver, CO 80210, USA
E-mail: salah.eltief@du.edu

Received: 19 May 2025; **Revised:** 18 September 2025; **Accepted:** 22 September 2025

Abstract: The primary objective of the control system in a half-bridge DC-DC buck converter is to maintain a constant output voltage through a feedback mechanism, regardless of input voltage or load variations. This paper presents a comparative analysis of several advanced control strategies, including Sliding Mode Control (SMC), Adaptive Sliding Mode Control (ASMC), and Fuzzy Adaptive Sliding Mode Control (FASMC), with a particular focus on optimizing ASMC and FASMC using Particle Swarm Optimization (PSO). The PSO algorithm is employed to fine-tune key controller parameters to mitigate chattering, improve transient response, and enhance overall system efficiency. Results demonstrate a significant reduction in steady-state output voltage ripple and improved stability under varying load conditions and line disturbances. The proposed converter and control strategies are evaluated across six distinct scenarios designed to assess performance under different operating environments. While all controllers were tested under identical conditions, ASMC and FASMC exhibited superior tracking capabilities. Among them, FASMC achieved the best overall performance in terms of response speed, chattering suppression, and energy efficiency. For benchmarking purposes, classical Proportional-Integral-Derivative (PID) and Model Predictive Control (MPC) methods were also implemented. However, these enhancements are specifically accomplished through the implementation of the FASMC control strategy, which efficiently mitigates the output voltage ripple and improves system stability.

***Keywords*:** half-bridge DC-DC converter, Sliding Mode Control (SMC), Adaptive Sliding Mode Control (ASMC), Fuzzy Adaptive Sliding Mode Control (FASMC), Particle Swarm Optimization (PSO)

1. Introduction

Half-bridge DC-DC converters serve as essential components in modern power electronics, playing a essential role in applications such as electric vehicles [1], renewable energy systems [2], and industrial power supplies [3]. Their primary objective is to convert a variable DC input voltage into a stable and regulated DC output, which is especially critical in systems where input voltages may vary significantly [4, 5]. Ensuring consistent and efficient output power is fundamental for the reliable operation of these systems [6]. However, maintaining voltage regulation under fluctuating load conditions and transient disturbances presents a major challenge. In this context, control algorithms become vital, as they determine the converter's ability to operate efficiently and stably. Selecting an appropriate control strategy is therefore key to optimizing performance, enhancing stability, and improving energy efficiency.

DOI: https://doi.org/10.37256/jeee.4220257262

The need for a regulated and stable output power in all high-performance and high-efficiency applications makes control algorithms in DC-DC power converters crucial. The main function of a control circuit in DC-DC converters is to guarantee stable and efficient operation by maintaining the desired output voltage, even in the presence of variations in input voltage, load conditions, and other disturbances [7–9]. Conventional control methods, such as PID and Proportional-Integral controllers as well as a pulse width modulation as a modulation technique, have been widely employed due to their simplicity and ease of implementation. However, these controllers often fall short in handling nonlinear system dynamics and load variations, leading to suboptimal performance and increased steady-state errors. To address these limitations, more advanced control strategies have been developed. SMC is known for its robust performance under harsh operating conditions. However, SMC faces a significant challenge known as chattering, which can lead to increased switching losses and Electromagnetic Interference (EMI).

ASMC and FASMC strategies have been developed to overcome the limitations of conventional SMC. These enhanced control strategies dynamically adapt their parameters to reduce chattering and improve system stability, making them more effective in handling parameter variations and external disturbances. However, their performance is highly sensitive to the precise tuning of multiple nonlinear control parameters, which is difficult to achieve using manual or classical tuning methods. To address the tuning challenge, PSO offers a promising solution due to its simplicity, fast convergence, and ability to handle nonlinear optimization problems. PSO is a population-based stochastic optimization method inspired by the collective behavior of bird flocking and fish schooling [10–12]. It has been successfully applied to tune the parameters of ASMC and FASMC, leading to enhanced tracking accuracy, reduced chattering, and improved energy efficiency. Although, PSO has proven to be a powerful tool for tuning DC-DC converter controllers, its application to fuzzy-enhanced sliding mode controllers in half-bridge converter topologies remains limited in the literature. Despite the advances introduced by ASMC and FASMC, parameter tuning continues to pose a challenge. PSO offers a promising solution by providing a systematic and adaptive optimization approach for fine-tuning control parameters, thereby achieving optimal tracking, minimal chattering, and enhanced energy efficiency [13].

Recent studies have explored the use of PSO in converter control. For example, [14] applied PSO to ASMC in bidirectional converters, while [15] focused on PSO-tuned PID control under load variations. These works demonstrate PSO's potential in controller tuning but are limited to simplified or linear topologies and predominantly time-domain evaluations. Despite the growing interest in optimization-based control, few studies have combined fuzzy logic, SMC, and PSO in the context of half-bridge converters. This work advances the field by introducing a PSO-tuned FASMC for half-bridge buck converters, integrating multi-level modeling and validating performance across dynamic, frequency, and energy domains. The proposed method specifically targets unidirectional half-bridge buck topology, enabling improved dynamic response, reduced chattering, and enhanced energy efficiency under varying conditions. The integration of fuzzy logic with PSO-tuned SMC optimizes control parameters and fine-tunes control actions, leading to more stable and efficient operation.

This manuscript focuses on optimizing control algorithms for half-bridge DC-DC converters using PSO, addressing existing research gaps and offering a comprehensive solution to prevailing challenges in this field. Despite progress in both control strategies and optimization methods, several key limitations remain. In particular, the integration of PSO with advanced techniques such as FASMC has yet to be thoroughly explored, and there remains a need for a structured and systematic approach to parameter tuning. This study aims to enhance system stability, efficiency, and dynamic response, ultimately contributing to the development of more reliable and high-performance power electronic systems by incorporating PSO with these advanced control approaches. A comprehensive comparative analysis of PID, SMC, ASMC, and FASMC controllers is conducted under a range of operating conditions. To thoroughly evaluate each control strategy, six distinct simulation scenarios were developed, each targeting a different aspect of controller performance to ensure a well-rounded assessment of their capabilities. Results confirm the efficacy of PSO-based tuning, with key outcomes including:

• Improved tracking accuracy: Optimized parameters enable faster and more precise tracking of reference signals, reducing steady-state errors.

• Reduced chattering: PSO mitigates high-frequency oscillations, lowering switching losses and EMI.

• Enhanced energy efficiency: Tuning through PSO improves overall system performance by reducing control effort and power loss.

This paper is organized into the following sections. Section 2 provides a review of relevant literature on DC-DC converter control strategies and optimization techniques. Section 3 presents the description and mathematical modeling of the half-bridge DC-DC converter. Section 4 details the implementation of various control strategies, including the integration of PSO with ASMC and FASMC. Section 5 outlines results discussion in both time and frequency domains and the simulation scenarios, evaluation metrics, and performance criteria. Finally, Section 6 concludes the paper and suggests possible directions for future work.

2. Literature review

Control circuits are designed to offer a fast response with minimal overshoot/undershoot and the ability to reject disturbances. In this context, selecting a suitable control algorithm and tuning methods improves device performance, but choosing the optimal tuning remains challenging, especially when managing several variables under various conditions [16, 17]. Numerous strategies for optimizing control parameters in half-bridge DC-DC converters have been proposed, ranging from conventional techniques to intelligent algorithms. PID controllers remain popular due to their simplicity and intuitive design process, and studies such as [18, 19] demonstrate their effectiveness in various power electronics applications. A PID and Pole Placement controller optimized by Genetic Algorithm (GA) was proposed in [20] for bidirectional half-bridge converters, though the study acknowledged residual chattering issues. Reference [21] introduced an anti-windup PID controller optimized via PSO, but limited its scope to conventional buck converters. Anti-windup strategies have also been explored for EV-integrated AC/DC systems [22], highlighting the importance of control robustness under power system disturbances. These conventional methods, while accessible, often fail under strong nonlinearities and load variation, leading to increased steady-state error and degraded dynamic performance.

To address these limitations, more advanced control strategies have emerged. MPC anticipates future behavior by solving an optimization problem over a finite horizon [23]. Its predictive power makes it robust to nonlinearity and external disturbances [24]. However, MPC requires accurate modeling and substantial computational power [25], making it less practical for real-time operation in embedded converters with limited resources. SMC, on the other hand, provides robustness against parameter variations and disturbances. It ensures convergence to a sliding surface and maintains system stability [26, 27]. However, a major drawback of SMC is chattering, caused by high-frequency switching actions [28, 29]. To mitigate this, researchers proposed ASMC and FASMC [30, 31], which dynamically adjust gains to reduce chattering while retaining robustness. Studies such as [32] demonstrate improvements in dynamic response and robustness, including variants like fixed-frequency SMC and fast terminal SMC. Additionally, recent studies, such as [33] and [34], have proposed novel approaches using fuzzy logic control combined with fast terminal sliding mode control and global fast terminal sliding mode control methods, respectively, to further enhance robustness performance and minimize power losses.

Optimization algorithms have become vital in tuning these advanced controllers**.** Among them, PSO stands out for its simplicity, convergence speed, and ability to avoid local optima in nonlinear settings [35]. While GA [36] and Simulated Annealing (SA) [37] have also been used, they often require more computational effort or fine-tuning of algorithm parameters. PSO offers an effective trade-off, requiring fewer parameters and enabling real-time tuning in constrained systems. Recent efforts such as [38] have combined PSO with Fractional-Order PID (FOPID) controllers in wide-bandgap-based boost converters to achieve improved efficiency in solar systems, demonstrating PSO's adaptability to advanced controller structures. Also, Work in [39] highlights the growing trend of using hybrid control and optimization strategies to enhance DC-DC converter performance in renewable systems, supporting the need for multi-layered control integration. PSO has been used to tune ASMC and FASMC controllers, improving tracking accuracy, reducing chattering, and enhancing energy efficiency [40, 41]. In control applications where precision and low power loss are critical, PSO-tuned controllers offer tangible benefits in tracking, stability, and reduced control effort [42]. Table 1 provides a comprehensive comparison of control strategies, summarizing their tuning methods, stability, and complexity.

Table 1. Comparison between control methods and their characteristics

Criteria	Control Method				
	PID	MPC	SMC	ASMC	FASMC
Tuning	Challenge always need trial & error. [43]	Systematic via model & cost weights [47]	Low sensitive to parameter variations [33]	Adaptive tuning minimizes manual intervention. [30]	Adaptive & fussy logic for effective dynamic tuning. [31]
Stability	Unsteady if properly untuned. [45]	High with model accuracy and constraints [48]	Robust to parameter changes & disturbances. [50]	Stability improved via adaptive mechanisms. [30]	Stability improved with fuzzy logic [53]
Response Time	Critical to balance response and the overshoot. [20]	Fast but depends on horizons [24]	Could be sensitive to noise but has fast response. [44]	Very fast response. [52]	Very high response with minimized overshoot. [31]
Chattering	Not a common issue [43]	None (uses smooth inputs) [25]	Can occur [33]	Minimized [40]	Minimal high frequency oscillations [53]
Handling Nonlinearities	Limited to linear systems [43]	Strong with accurate nonlinear model [23]	Robust [49]	Enhanced to nonlinearities [40]	highly robust [36]
Disturbance Rejection	Effective [20]	Strong, anticipates future errors [48]	Excellent [33]	Improved [52]	The best [54]
Complexity & Implementation	Quite simple & easy to implement [46]	High (modeling + online optimization) [49]	Complex [51]	More complex [30]	Most complex [55]

Consequently, the control circuits for half-bridge DC-DC converters highlights the need for fast, accurate responses and robust disturbance rejection. Conventional methods like PID controllers are simple but struggle with nonlinearities and load variations, leading to increased errors and degraded performance. Advanced strategies such as MPC and SMC offer better robustness and dynamic response but face challenges like high computational requirements and chattering. To address these issues, this work introduces a PSO-tuned fuzzy-adaptive SMC for unidirectional isolated converters. By integrating multi-level modeling and validating performance across dynamic, frequency, and energy domains, the proposed method improves dynamic response, reduces chattering, and enhances energy efficiency under varying conditions. This approach fills a critical gap in the literature, providing a robust and practical solution for real-time control in embedded systems with limited resources.

3. Description and mathematical modeling of the proposed converter

The half-bridge DC-DC converter is an efficient power conversion topology designed to step up or down a DC input voltage to a lower or higher DC output voltage. This section presents a detailed system description and mathematical modeling of the proposed converter. To model the converter accurately, it is important to understand its key components and their interconnections. The mathematical model, in turn, is essential for analyzing both the steady-state and dynamic behavior of the system, thereby facilitating accurate control design and parameter optimization [56]. Additionally, a comprehensive analysis, including graphical evaluation of the system's performance, is carried out.

3.1 *Proposed converter description*

The half-bridge DC-DC converter is a widely used power conversion topology that efficiently converts a DC input voltage into a lower or higher DC output voltage. A basic half-bridge DC-DC converter circuit configured as a buck

converter is illustrated in Figure 1. The proposed topology analyzed in this study is based on designs reported in [57]. The system consists of two primary components: (1) two regulation switching transistors (typically SiC MOSFETs), and (2) a resonant tank circuit. The resonant stage includes a high-frequency transformer, two relatively large capacitors C1 and C2, a magnetic inductor Lm, and a leakage inductor Lk on the input side. On the output (rectifier) side, the converter incorporates an inductor L and a filter capacitor C3 to smooth the output voltage.

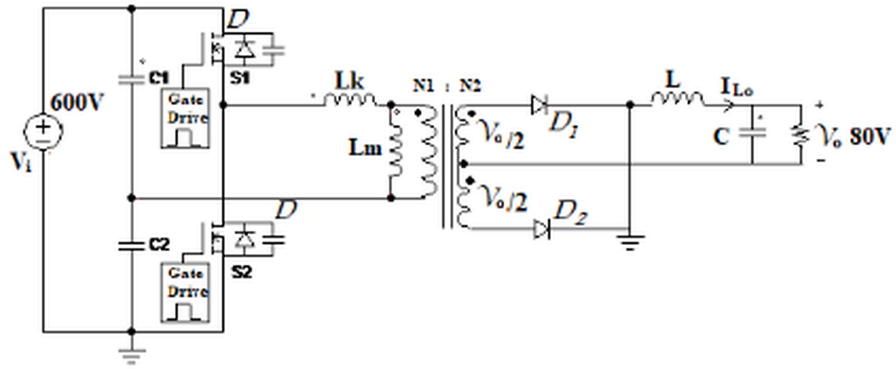

Figure 1. Schematic of the half-bridge buck converter. C_3 (output capacitor), i_L (inductor current), v_C (capacitor voltage), N_p (primary turns), N_s (secondary turns)

3.1.1 *High-frequency transformer*

The transformer in the proposed converter is specifically designed to operate at high frequencies. High-frequency operation enables the use of smaller and lighter transformers, which is crucial for reducing the overall size and weight of the system. It is important to select a transformer core that is compact, lightweight, and exhibits low core losses [58]. For high-frequency applications, an iron-based nanocrystalline soft-magnetic core (FT-3KM material) is selected. This material is preferred over ferrite cores due to its higher saturation magnetic flux density, greater magnetic permeability, superior thermal stability, and reduced core losses. The winding configuration is optimized to minimize conduction and proximity losses and to ensure efficient power transfer [59].

3.1.2 *Output filter description*

The output filter is a critical component responsible for smoothing the output voltage and current, thereby minimizing voltage ripple and high-frequency noise. The filter typically consists of an inductor and capacitor arranged in series. The inductor stores energy during the on-time of the switches and releases it during the off-time, while the capacitor attenuates high-frequency switching components.

The output inductor (L) smooths the current flowing to the load and can be expressed as:

$$L = \frac{V_o \cdot (1 - D)}{f_{sw} \cdot \Delta I_o} \tag{1}$$

where ΔI_o is the acceptable current ripple on the output side, (V_o) is the output voltage, (f_{sw}) is the switching frequency, and (D) is the duty cycle. The value of the inductor should be adjusted based on the desired ripple, load current, and switching frequency.

The capacitors (C_1) and (C_2) connected to the switching leg, often referred to as decoupling or bypass capacitors, play a significant role in the converter's operation. These capacitors help maintain a stable voltage across the switches and the transformer, thereby reducing voltage stress and improving overall system reliability. They also assist in filtering out

high-frequency noise and ensure that the switches operate within their safe operating area. The required capacitance on the primary side, which forms the midpoint of the half-bridge configuration, can be estimated as:

$$C_1 = C_2 = \frac{P_o}{2f_{sw} \cdot \Delta V \cdot V_i} \tag{2}$$

Where P_o is the output power delivered to the load, f_{sw} is the switching frequency, and ΔV is the allowable voltage ripple across the capacitors,

3.2 *Mathematical modeling*

An accurate mathematical modeling is a significant for designing and optimizing the converter's operation under a wide range of input and load conditions. The inclusive mathematical modeling of a half-bridge buck converter is critical for understanding its three fundamental steps: first, define the switching model, then, derive a continuous time averaged model, finally, obtain a steady state operating point and linearized model to enable accurate control design and optimization [60]. As established by [61], the essential operation of the half bridge converter is defined by the fact that the transformer primary voltage $v_{T(t)}$ is then (0.5 Vgs) when transistor S1 conducts, and (-0.5 Vgs) when transistor S2 conducts. This key insight directly leads to the factor of 0.5 in its DC gain and is the starting point for developing its switched and averaged models. In this section, we present the modeling of the proposed converter, focusing in critical elements including switching model, average model, steady state analysis and reduced order control model.

3.2.1 *Switching model*

The proposed half bridge converter alternates between four topological modes within each switching cycle of period Ts. During each switching cycle of period T_s, the switches operate with a duty cycle D, applying alternating square-wave voltages of amplitude $V_i/2$ across the transformer. The rectified secondary waveform produces a unipolar pulse with an effective amplitude of $V_i/(2n)$, where $n = N_p/N_s$ is the turns ratio. Assuming Continuous Conduction Mode (CCM) and ideal switching. To analyze dynamic behavior, a state space averaged model is constructed, and the state vector is expressed as:

$$x(t) = \begin{bmatrix} i_L(t) \\ \\ v_C(t) \end{bmatrix} \tag{3}$$

where $i_L(t)$ is the inductor current and $v_C(t)$ is the voltage across the output filter capacitor (approximately equal to the output voltage v_o).

The system can be described by a set of linear state space equations that change with the switch configurations:

$$\dot{x}(t) = A_n x(t) + B_n u(t), \quad u(t) = V_i, \quad \text{for} \quad n = 1,2,3,4 \tag{4}$$

where $u(t) = V_i$ is the input voltage, and n denotes the operating mode as follows:

Mode 1: During this phase, the upper switch S_1 is turned ON while diode D_2 conducts on the secondary side. The input voltage V_i is applied across half of the transformer primary winding ($\frac{V_i}{2}$), which induces a secondary voltage of $\frac{V_i}{2n}$. Energy is transferred from source to load through the output filter.

$$\dot{x} = A_1 x + B_1 V_i = \frac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix} V_i \tag{5}$$

Mode 2: When both switches are OFF during dead-time, the inductor current freewheels through the upper diode D_1. The transformer primary voltage collapses to zero, and the output filter maintains.

$$\dot{x} = A_2 x + B_2 V_i = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i \tag{6}$$

Mode 3: In this complementary active phase, lower switch S_2 conducts while diode D_1 on the secondary side becomes forward biased. The transformer primary sees $\left(-\frac{V_i}{2}\right)$, producing $\left(-\frac{V_i}{2n}\right)$ on the secondary while maintaining power flow direction.

$$\dot{x} = A_3 x + B_3 V_i = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} - \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix} V_i \tag{7}$$

Mode 4: During the complementary dead-time period, the inductor current freewheels through lower diode D_2. This mode mirrors Mode 2 but with opposite diode polarity, maintaining current continuity during switching transitions.

$$\dot{x} = A_4 x + B_4 V_i = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i \tag{8}$$

The system matrices for all modes are therefore:

$$A_1 = A_2 = A_3 = A_4 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, \quad B_1 = \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix}, B_2 = B_4 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, B_3 = \begin{bmatrix} -\frac{1}{2nL} \\ 0 \end{bmatrix}$$

Figure 2 illustrates the gate signals, transformer voltages, and key currents defining these four modes.

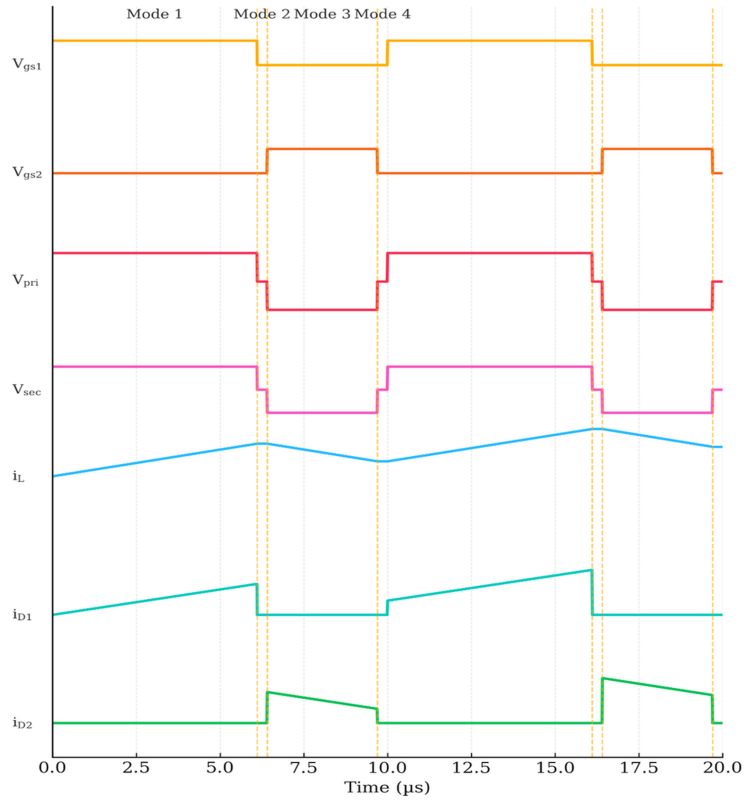

Figure 2. Four mode waveforms showing gate signals (V_{gs1}, V_{gs2}), primary and secondary voltages (V_{pri}, V_{sec}), inductor current (i_L), and diode currents (i_{D1}, i_{D2}). Modes 1 and 3 are active phases, while Modes 2 and 4 represent dead times. $V_{pri} \in \left\{+\frac{V_i}{2}, 0, -\frac{V_i}{2}\right\}$ and $V_{\text{sec}} \in \left\{+\frac{V_i}{2n}, 0, -\frac{V_i}{2n}\right\}$.

3.2.2 *State-space averaged model*

The state space average method is applied to estimated the switched system with a continuous time model. The duty cycle is defined as the fraction of the period for which each active switch is on. For complementary operation with duty cycles less than 0.5, the fractional times spent in each mode are: ($d_1 = D$ in mode 1), ($d_2 = (0.5 - D)$ in mode 2), ($d_3 = D$ in mode 3) and ($d_4 = (0.5 - D)$ in mode 4)

The averaged system matrices are calculated as the duty weighted sum

$$A = d_1A_1 + d_2A_2 + d_3A_3 + d_4A_4 \tag{9}$$

$$B = d_1B_1 + d_2B_2 + d_3B_3 + d_4B_4 \tag{10}$$

Substituting the matrices:

$$A = (\ D + (05 - D) + D + (0.5 - D)) \cdot \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{11}$$

$$B = D \cdot \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix} + (0.5 - D) \cdot \begin{bmatrix} 0 \\ 0 \end{bmatrix} + D \cdot \begin{bmatrix} -\frac{1}{2nL} \\ 0 \end{bmatrix} + (0.5 - D) \cdot \begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{12}$$

The standard averaging yields ($B = 0$), indicating that the input voltage (V_i) does not directly appear in the averaged dynamics. This is a known result for symmetrical bridge converters; the effective control input is the product of the duty cycle and input voltage, $(D(t), V_i)$. The correct averaged model is:

$$\dot{x}(t) = A_n x(t) + B_d \cdot (D(t)\, V_i) \tag{13}$$

where $B_d = \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix}$ is derived from the combined effect of the active phases. Thus, the final continuous time averaged state space model becomes:

$$\dot{x}(t) = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} x(t) + D(t) \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix} V_i \tag{14}$$

This model captures the essential converter dynamics, excluding high-frequency switching ripple, and is suitable for linear controller design.

3.2.3 *Steady-state analysis*

The steady state operating point (X, D) is found by setting the derivative in the averaged model to zero:

$$0 = Ax + B_d \cdot D \cdot V_i \tag{15}$$

Solving for the state vector X = [I_L , V_o]$^{\mathrm{T}}$:

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L \\ V_o \end{bmatrix} + D \begin{bmatrix} \frac{1}{2nL} \\ 0 \end{bmatrix} V_i \tag{16}$$

From the first equation:

$$0 = 0 \cdot I_L - \frac{V_o}{L} + \frac{V_i}{2nL} D \quad \Rightarrow \quad V_o = \frac{V_i}{2n} D \tag{17}$$

From the second equation:

$$0 = \frac{I_L}{C} - \frac{V_o}{RC} + 0 \quad \Rightarrow \quad I_L = \frac{V_o}{R} \tag{18}$$

The DC voltage transfer function is therefore:

$$M_v = \frac{V_o}{V_i} = \frac{D}{2(\frac{N_s}{N_p})} = \frac{1}{2} D \cdot \frac{N_s}{N_p} \tag{19}$$

3.2.4 *Reduced order control model*

For control-oriented modeling, a reduced-order formulation is employed based on the output voltage. Let $x_1 = v_o$ represent the output voltage and $x_2 = \dot{v}_o$ its time derivative. The state vector is defined as:

$$x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} v_o \\ \dot{v}_o \end{bmatrix} \tag{20}$$

The system dynamics are expressed as:

$$\dot{x} = Ax + Bu \tag{21}$$

where the matrices are:

$$A = \begin{bmatrix} 0 & 1 \\ -\frac{1}{Lc}\left(1 + \frac{L}{RC}\right) & -\frac{1}{Rc} \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \frac{1}{L} \cdot \frac{N_s}{N_p} V_i \end{bmatrix}, \quad u = d(t) \tag{22}$$

Here, A represents the system dynamics, and B captures the effect of the duty cycle input $d(t)$ on the state evolution. This representation is used for controller synthesis in sliding mode frameworks.

3.3 *Sliding Mode Control*

SMC is widely used in power converters due to its robustness, fast response, and strong disturbance rejection capabilities. SMC is designed to handle nonlinearities, uncertainties, and external disturbances [62]. However, conventional SMC suffers from chattering, which can lead to excessive switching losses and stress on power components. To address these limitations, two enhanced SMC variants are introduced. The sliding surface is defined as:

$$\phi = Cx = \lambda_1 x_1 + x_2 = \begin{bmatrix} \lambda_1 & 1 \end{bmatrix} x \tag{23}$$

where C is the coefficient matrix, and λ_1 is the sliding surface gain.

The derivative of the sliding surface is:

$$\dot{\phi} = C\dot{x} = C(Ax + Bu) \tag{24}$$

Setting $\dot{\phi} = 0$ for equivalent control:

$$0 = C(Ax + Bu_{eq})$$
$$\Rightarrow u_{eq} = -(CB)^{-1}CAx \tag{25}$$

Substitute matrices :

$$CB = \begin{bmatrix} \lambda_1 & 1 \end{bmatrix} B = \frac{1}{Lc} \cdot \frac{N_s}{N_p} V_i \tag{26}$$

$$\begin{aligned} CA &= \begin{bmatrix} \lambda_1 & 1 \end{bmatrix} \begin{bmatrix} 0 & 1 \\ -\frac{1}{Lc}\left(1 + \frac{L}{Rc}\right) & -\frac{1}{Rc} \end{bmatrix} \\ &= \begin{bmatrix} -\frac{1}{Lc}\left(1 + \frac{L}{Rc}\right) & \lambda_1 - \frac{1}{Rc} \end{bmatrix} \end{aligned} \tag{27}$$

Then

$$u_{eq} = -\left(\frac{Lc \cdot N_p}{N_s \cdot V_i}\right)\left[-\frac{1}{Lc}\left(1 + \frac{L}{Rc}\right)x_1 - \left(-\lambda_1 + \frac{1}{R}\right)x_2\right] \tag{28}$$

The total control input becomes:

$$d(t) = u_{eq} + \lambda_2 \tanh(\phi) \tag{29}$$

where u_{eq} is the equivalent control that enforces the sliding condition, λ_2 is the switching gain, and $tanh(\phi)$ provides a smooth switching action based on the sliding surface ϕ.

3.4 *Adaptive Sliding Mode Control*

While conventional SMC provides robustness and fast response, it suffers from high-frequency chattering, which may lead to increased switching losses and component stress. To address these issues, an adaptive extension, ASMC is introduced. ASMC dynamically adjusts the switching gain to enhance adaptability [63]. It adapts its parameters in real-time to effectively handle model uncertainties and operating condition variations. To improve robustness and convergence, a modified sliding surface is introduced:

$$\sigma = \phi + \gamma \tanh(\phi) \int_0^t \phi(\tau) d\tau \tag{30}$$

The control law in ASMC includes an adaptive gain λ_2, which evolves based on a defined adaptation rule:

$$d(t) = u_{eq} + \lambda_2 \cdot \tanh(\sigma) \tag{31}$$

where λ_2 is a time-varying extension of the constant gain used in conventional SMC, dynamically adapted to enhance performance, and u_{eq} represents the corresponding equivalent control, given by:

$$u_{eq} = \frac{LcN_p}{N_s V_i(t)} \left[\left(\lambda_1 + \gamma - \frac{1}{Rc} \right) x_2 + \gamma \lambda_1 x_1 + \frac{v_o(t)}{Lc} \right] \tag{32}$$

3.5 *Fuzzy Adaptive Sliding Mode Control*

FASMC builds on the adaptive principles of ASMC by embedding a fuzzy logic controller, enabling more nuanced and intelligent adjustment of the switching gain. This integration combines the strengths of fuzzy logic and adaptive sliding mode control, offering improved handling of complex nonlinear dynamics and enhancing robustness across a wider range of operating conditions [64]. To further reduce chattering and enhance adaptability, a Fuzzy Inference System (FIS) is applied to dynamically tune the switching gain based on the sliding surface and its derivative:

$$\mathbf{u}_{fuzzy} = \begin{bmatrix} \phi \\ \dot{\phi} \end{bmatrix}, \quad \lambda_f = \mathrm{FIS}(\mathbf{u}_{fuzzy}) \tag{33}$$

Where $\mathbf{u}_{fuzzy}$ is the input vector to the FIS, λ_f is fuzzy tuned gain determined by a fuzzy inference system.

The fuzzy controller adjusts the gain based on the system's current state to accelerate convergence when far from the sliding surface and decreases switching intensity near equilibrium. The rule base as shown in Table 2 is constructed with three linguistic levels: Negative (N), Zero (Z), and Positive (P) for both inputs. The output gain levels are Low (L), Medium (M), and High (H).

Table 2. Rule table

$\phi \backslash \dot{\phi}$	N	Z	P
N	H	M	L
Z	M	L	M
P	L	M	H

The adaptive gain output from the fuzzy system is used in the control signal:

$$d(t) = u_{eq} + \lambda_f \cdot \tanh(\sigma) \tag{34}$$

This strategy achieves a smoother control response, mitigates chattering, and maintains strong tracking and robustness characteristics under dynamic conditions.

4. Particle Swarm Optimization

Adaptive and fuzzy-based sliding mode controllers (SMC, ASMC, and FASMC) are designed to improve robustness and mitigate chattering; however, their performance is highly dependent on accurate parameter tuning. PSO offers a systematic and intelligent approach to refining these parameters, ensuring optimal dynamic performance [65]. PSO is a population-based optimization algorithm that searches for the best solution within a defined space. In this study, PSO is employed to optimize the control parameters of SMC, ASMC, and FASMC, thereby enhancing stability, reducing chattering, and improving voltage regulation. Its capability to efficiently explore the parameter space makes PSO a highly effective tool for tuning controllers in complex dynamic systems.

The objective function for PSO minimization includes key tracking performance metrics:

• Integral Absolute Error (IAE).

• Integral Squared Error (ISE).

• Rise time and settling time.

The set of parameters optimized for each:

• SMC: Sliding surface gain $\lambda 1$ and switching gain $\lambda 2$,

• ASMC: Sliding surface gain $\lambda 1$, switching gain $\lambda 2$, and adaptive gain γ,

• FASMC: Sliding surface gain $\lambda 1$, adaptive gain γ, and fuzzy tuned gain λ_f.

The optimization issue is solved offline, where PSO searches the parameter space by evaluating a swarm of particles iteratively. Each particle adjusts its position based on its own experience and the experience of neighboring particles:

$$v_i(t+1) = wv_i(t) + c_1 r_1 \left(p_i^{best} - p_i(t)\right) + c_2 r_2 \left(g - p_i(t)\right) \tag{35}$$

$$p_i(t+1) = p_i(t) + v_i(t+1) \tag{36}$$

where $p_i(t)$ and $v_i(t)$ are the position and velocity of particle i at iteration t, respectively; p_i^{best} is the best position found by particle i; and g is the global best position found among all particles. The term ω is the inertia weight that balances exploration and exploitation. The constants c_1 and c_2 are the cognitive and social acceleration coefficients, controlling the influence of the particle's own experience and that of the swarm. The variables r_1 and r_2 are random numbers drawn from a uniform distribution in the range $[0, 1]$, introducing stochastic behavior into the search process.

When optimized, the parameters are integrated into the control laws, improving system stability, minimizing steady-state error, and enhancing transient response.

4.1 *Fitness function for controller optimization*

The optimization method is directed by a fitness function which simultaneously promotes tracking accuracy, dynamic responsiveness, and reduced control effort. The fitness function is defined as:

$$J = \sum_{t=0}^{T} \left(\alpha |e(t)| + \beta |\phi(t)| + \theta |d(t)|\right) \tag{37}$$

Where: $e(t) = V_{ref} - V_o(t)$, voltage tracking error, $\phi(t)$ sliding surface, $d(t)$ the total duty cycle, and α, β, θ are weighting factors for accuracy, stability, and control smoothness.

4.2 *Optimization results*

4.2.1 *PSO convergence*

The PSO algorithm was used to tune the controller parameters for SMC, ASMC, and FASMC, optimizing the sliding surface, control gains, adaptive laws, and fuzzy logic rules to ensure superior performance. PSO convergence indicates that the particles move toward the best solution, confirming finely tuned controllers. The optimization aimed to minimize a composite cost function combining IAE, ISE, and control effort, ensuring fast dynamic response, precise voltage tracking, and smooth duty cycle behavior. The optimized parameters are summarized in Table 3.

Table 3. Optimized controller parameters obtained using PSO

Controller	Optimized λ_1	Optimized λ_2/λ_f	Optimized γ
SMC	3.50	15.00	–
ASMC	3.75	13.5	22.00
FASMC	4.00	Fuzzy-tuned (initial 12.5)	20.00

The PSO was configured with 30 particles and a maximum of 30 iterations, achieving convergence within 20 iterations for all controllers. Figure 3 illustrates the steady reduction in the cost function value, demonstrating the efficiency and robustness of the PSO approach.

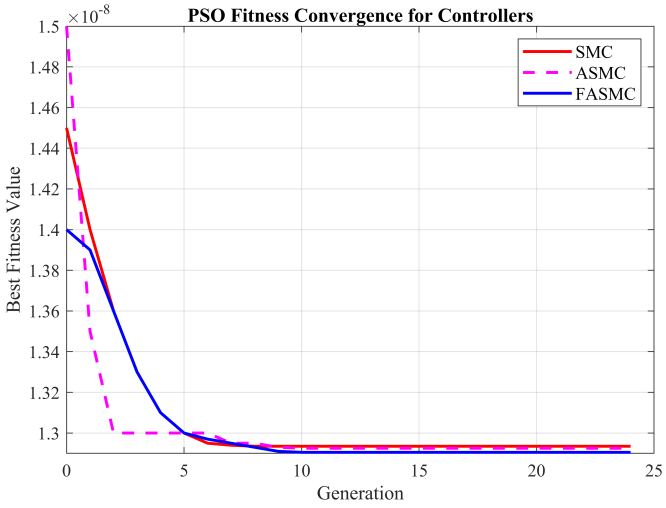

Figure 3. PSO fitness function convergence over iterations

4.2.2 *Step response comparison*

The step response of each controller is illustrated in Figure 4, providing a comparative analysis of their performance. The SMC controller shows a fast initial response, reaching about 60 V in the first 10 ms, but with noticeable oscillations before stabilizing. The ASMC strategy improves on this by minimizing overshoot and oscillations, offering a smoother transition to the desired output voltage. The FASMC strategy achieves the best balance, with a fast response, minimal overshoot, and negligible chattering, demonstrating superior voltage regulation. This comparison highlights the progressive enhancements in control strategies, with FASMC providing the most stable and controlled response.

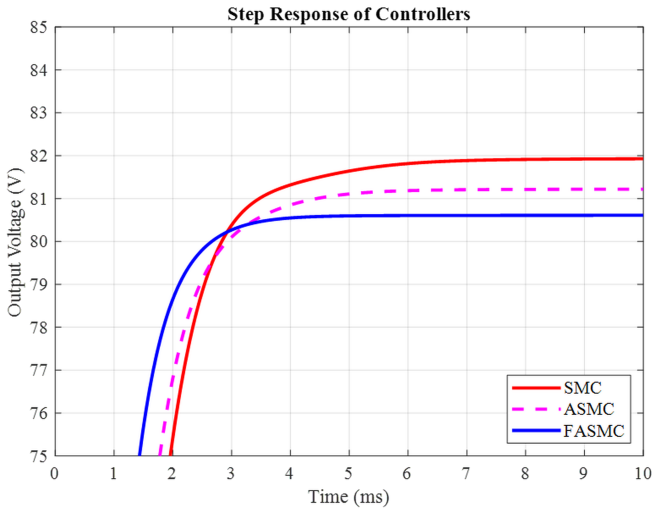

Figure 4. Step response comparison of various control strategies

Consequently, the performance metrics of each controller summarized in Table 4. The results ensure that FASMC method outperforms all other controllers in terms of fast response, minimal chattering, and high efficiency.

Table 4. Performance comparison of selected control strategies

IController	Rise Time	Settling Time	Overshoot	Steady-State Error	Control Effort	Fitness Convergence
SMC	~1.8 ms	~3.2 ms	Medium (~3%)	Low (~0.3 V)	Moderate (initial peaks)	Fast early drop, stable
ASMC	~1.5 ms	~2.6 ms	Low (~1.8%)	Very Low (~0.2 V)	Moderate, smoother	Steady convergence
FASMC	~1.1 ms	~2.0 ms	Very Low (<1%)	Negligible (<0.1 V)	Low, stable	Fastest, best

4.2.3 *Control effort analysis*

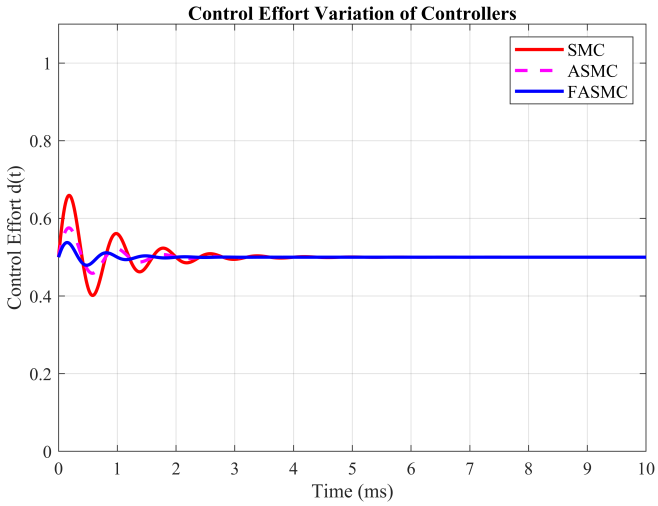

Figure 5. Control effort comparison of SMC, ASMC, and FASMC strategies

The control effort ($d(t)$) for all control strategies is compared in Figure 5. Over a 10 ms period, the SMC controller shows a high initial control effort with high-frequency switching, which can lead to oscillations. The ASMC strategy smooths the control action, starting at 0.8 and decreasing to 0 over the period, minimizing oscillations and providing a more stable and efficient effort. The FASMC strategy demonstrates the most effective control effort, with a smooth and balanced response and minimal chattering, thanks to its fuzzy logic component. In summary, while SMC provides a rapid but aggressive response, ASMC adapts to system dynamics for smoother control, and FASMC delivers the most refined and adaptive control effort, making it the superior choice.

5. Results discussion

The primary objective in designing a DC-DC converter is to optimize key parameters such as size, weight, cost, efficiency, and reliability. Considering these factors, appropriate components are selected to build a converter tailored to the specific application. To validate the proposed half-bridge DC-DC converter, a simulation model with a 600 V input was developed using MATLAB/Simulink. The system parameters are summarized in Table 5.

Table 5. Parameters of the proposed converter

Parameters	Symbol	Value	Unit
Input voltage (max & min)	v_i	600	V
Nominal output voltage (max & min)	v_o	80	V
Duty ratio	D	0.45–0.5	%
Switching frequency (max & min)	fsw	100	kHz
Power rating	P_o	400	W

Designing a half-bridge converter for stepping down from 600 V to 80 V requires precise component sizing. The two main switching devices on the primary side, S1 and S2, along with their body diodes D1 and D2, are driven by complementary control signals to prevent simultaneous conduction and avoid short circuits. When S1 conducts and S2 is off, the input voltage v_i is applied to one side of the transformer's primary winding. Conversely, when S2 conducts and S1 is off, the opposite polarity is applied, resulting in a square-wave voltage across the transformer. On the secondary side, the alternating voltage is rectified using two diodes, converting it into pulsating DC. A filter stage, composed of capacitors and inductors, smooths the output to deliver a stable DC voltage. The theoretical waveforms for the buck-mode operation of the proposed converter are detailed in [61, 62]. The output voltage is regulated by adjusting the duty cycle of the switching transistors as part of the control strategy.

5.1 *Scenarios*

In this work, a comprehensive simulation conducted to evaluate the performance of control methods used in half-bridge DC-DC buck converter including: PID, MPC, SMC, ASMC, and FASMC. These controllers are simulated by MATLAB Simulink software and tested under various challenging scenarios to identify their strengths and weaknesses of each control method, and providing valuable insights for choosing the most suitable controller. This evaluation focus on key performance indicators such as response time, overshoot, and settling time, and to determine the robustness, stability, and efficiency of each controller.

1) Step reference tracking

Step reference tracking evaluates the controllers dynamic response and regulation accuracy of each controller when the reference voltage (vref) changes from 80 V to 100 V at (t = 2.5) ms. Figure 6 shows the output voltage responses of the controllers. The PID controller has a gradual rise with significant overshoot and oscillations, indicating poor transient response. SMC improves speed and robustness but exhibits chattering and minor overshoot. ASMC reduces overshoot

and chattering, offering faster and more stable convergence than PID and SMC. FASMC, incorporating fuzzy logic for adaptive gain tuning, achieves the fastest and most stable tracking with negligible overshoot and minimal chattering. MPC also performs well, with smooth voltage tracking and minimal overshoot, though it is slightly slower due to computational delays. All controllers stabilize around 100 V within 3.5 - 4.0 ms, but FASMC and MPC outperform the others, with FASMC demonstrating the best transient performance. These results highlight FASMC's suitability for high-performance DC-DC converter applications requiring fast, precise, and stable voltage regulation.

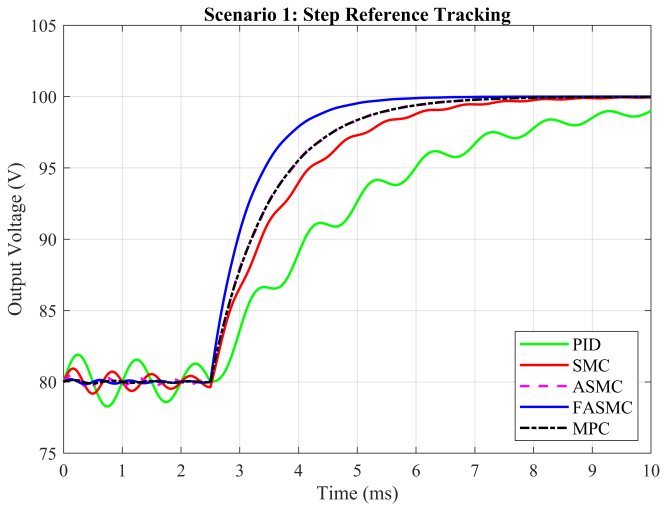

Figure 6. Output voltage response under step change in reference (80 V to 100 V @ 25 ms)

2) Load resistance change

The ability of a controller to maintain output voltage stability during sudden load resistance changes is a key indicator of its robustness and dynamic regulation capability. In this scenario, a step disturbance at (t = 0.5) ms simulates a sudden drop in load resistance. Figure 7 shows the output voltage responses of five controllers. The PID controller reacts slowly, with a noticeable voltage drop to approximately 79 V and some fluctuation before recovery. The SMC responds more quickly, with reduced steady-state error and faster recovery, but still shows visible voltage ripple and minor overshoot. The ASMC improves performance with dynamic gain adjustment, resulting in a smoother response and quicker stabilization, with a slight drop to around 79.2 V. The FASMC delivers the best dynamic performance, showing minimal voltage drop, rapid recovery, and excellent suppression of oscillations and overshoot, with negligible chattering. The MPC offers a smooth and stable response, closely matching the reference voltage after a modest drop, though with slightly more delay than FASMC. These results emphasize the superiority of advanced nonlinear and predictive control strategies in maintaining voltage stability under abrupt load disturbances.

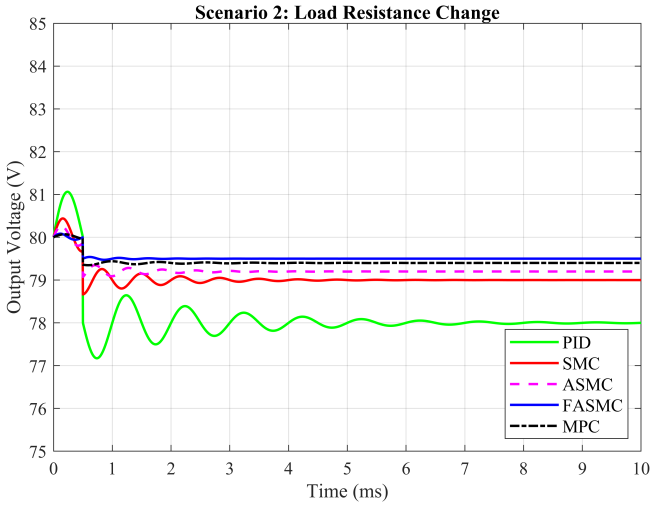

Figure 7. Output voltage response under a step change in load resistance

3) Input voltage drop

This scenario evaluates the robustness of each controller when the input voltage experiences a sudden drop at (t = 5) ms. Figure 8 illustrates the output voltage responses of the controllers under this disturbance. The objective is to maintain a regulated output voltage despite fluctuations in the input supply. The PID controller shows significant oscillations and limited disturbance rejection, with the output voltage fluctuating between 79.6 V and 81.3 V. The SMC controller performs better, with reduced ripple and faster recovery, but chattering is still present. The ASMC controller further improves voltage regulation by dynamically adjusting its gains, resulting in lower oscillations and a quicker return to steady-state. The FASMC achieves the best performance, maintaining the output voltage with minimal ripple, no visible chattering, and fast recovery, highlighting its superior disturbance rejection and dynamic stability. The MPC controller also offers a smooth and stable response, effectively handling the voltage drop with a modest dip and gradual recovery, though its convergence is slightly slower than FASMC due to its horizon-based optimization.

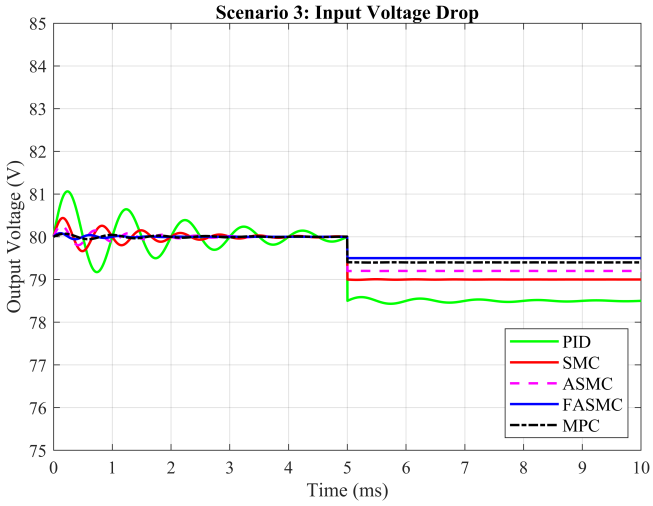

Figure 8. Output voltage comparison under an input voltage drop for various controllers

4) Initial condition perturbation

Initial condition perturbation assesses each controller's ability to recover from a non-ideal starting state. Figure 9 shows the output voltage responses of the control strategies when the system is initialized with a −3 V voltage offset below the reference. The PID controller exhibits the slowest recovery, remaining below the reference even after 7.5 ms, indicating poor compensation for initial disturbances. The SMC controller recovers faster, reaching steady-state around 4 ms, but shows chattering and moderately aggressive control action. The ASMC controller provides a smoother response with adaptive gain adjustment, minimizing oscillations and overshoot, and recovering more efficiently. The MPC controller also handles the offset effectively, offering a clean and stable trajectory to the reference, though it is slightly slower than FASMC due to its predictive model. The FASMC achieves the best performance, with the fastest and most stable recovery, minimal steady-state error, and negligible chattering, confirming its superior transient and regulation capabilities.

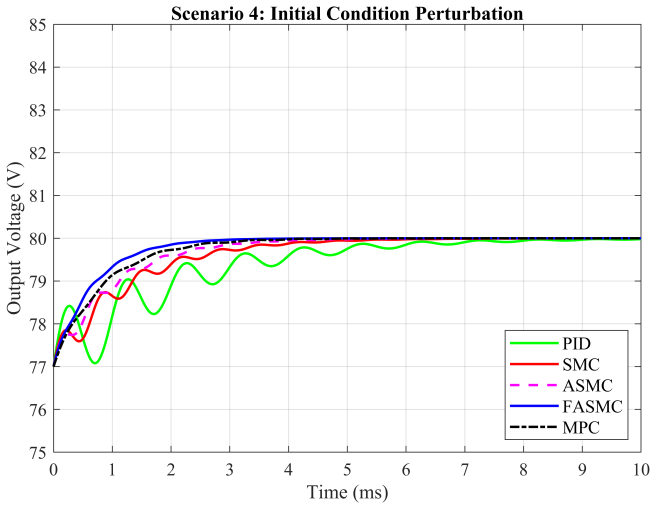

Figure 9. Output voltage comparison under initial condition perturbation for controllers

5) Load disturbance rejection

Load disturbance rejection evaluates a controller's ability to maintain output voltage stability during sudden load changes. In this scenario, a step load disturbance is introduced at ($t = 0.3$) ms, and the system's dynamic response is analyzed. Figure 10 presents the output voltage trajectories of the selected controllers under identical disturbance conditions. The PID controller shows the largest voltage deviation, with a pronounced undershoot and slow recovery, highlighting its limited robustness and weak transient performance. The SMC controller performs better, with a faster response and improved disturbance rejection, but chattering is still evident. The ASMC controller further enhances performance by dynamically tuning its gains, reducing overshoot and chattering, and achieving faster convergence and better voltage regulation. The MPC controller also demonstrates excellent rejection capability, achieving a well-regulated, ripple-free output with minimal overshoot, though its response is slightly slower than FASMC. The FASMC delivers the best performance, with minimal overshoot, negligible steady-state error, and a rapid, smooth transition, virtually eliminating chattering.

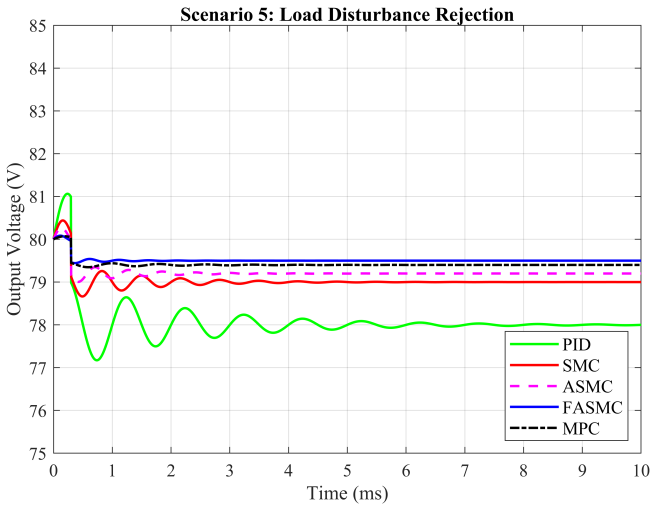

Figure 10. Output voltage response of controllers under load disturbance

6) Noisy reference tracking

This scenario evaluates each controller's ability to track a reference voltage signal contaminated with high-frequency noise, aiming to minimize output deviations and maintain stability. Figure 11 shows the responses of the control methods under a noisy reference signal. The PID controller is the most sensitive to noise, exhibiting significant ripple and erratic performance. The SMC controller shows improved noise robustness but still experiences visible oscillations and chattering. The ASMC controller outperforms both by adaptively tuning its gains, reducing chattering and improving stability. The FASMC achieves the best performance, with excellent tracking accuracy, minimal ripple, and strong noise suppression, making it ideal for high-precision applications. The MPC controller also performs well, delivering a clean and stable output with minimal ripple, though its response is slightly slower than FASMC due to predictive horizon computations.

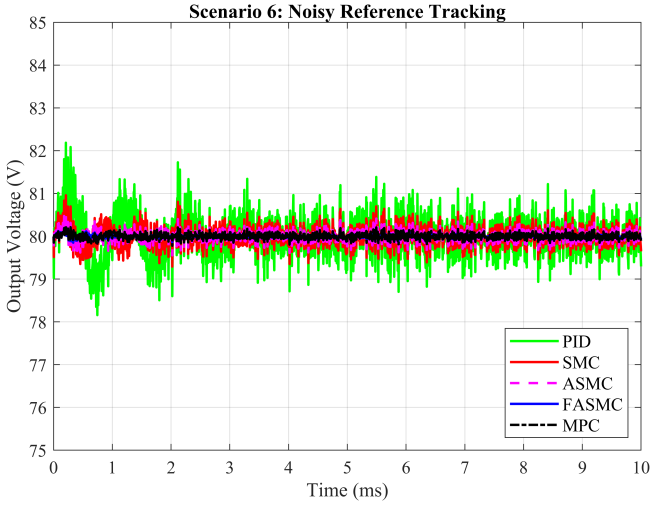

Figure 11. Output voltage response of different controllers under a noisy reference signal

5.2 *Frequency-domain stability analysis*

To assess the stability and robustness of each control strategy, frequency-domain analysis using Bode plots and margin extraction was performed. Figure 12 shows the Bode plots of the open-loop systems for PID, SMC, ASMC, FASMC, and MPC controllers, revealing significant variations in stability margins and bandwidth. The PID controller has the narrowest phase and lowest gain margins, indicating poor robustness to modeling uncertainties and system delay. The SMC controller shows improved phase margin and bandwidth, reflecting better dynamic behavior but remains sensitive to noise, causing chattering. The ASMC controller offers increased phase and gain margins, leading to faster response and better rejection of perturbations, confirming its adaptive advantages. FASMC demonstrates the most robust performance with the highest phase margin (above 60°) and strong gain margin, aligning with its superior time-domain performance. The MPC controller performs similarly to FASMC, with slightly lower bandwidth but smooth roll-off and strong phase stability, matching its reliable and stable tracking response in simulations.

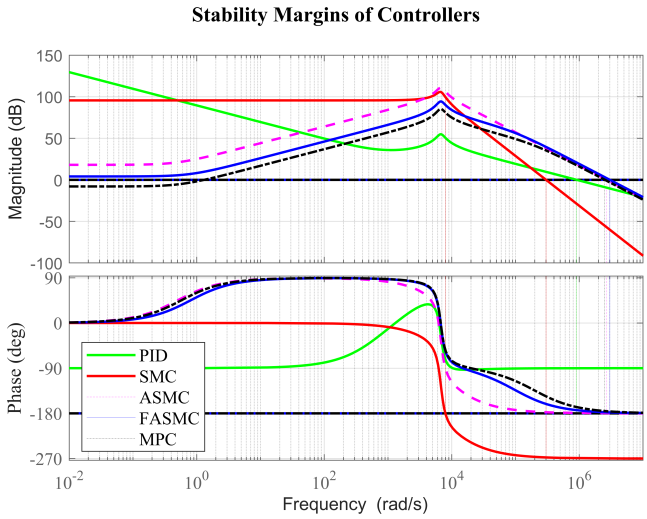

Figure 12. Bode plots of the open-loop systems for the five controllers

5.3 *Efficiency analysis*

Efficiency is a critical performance metric in power electronics, reflecting how effectively input power is converted into useful output power. Figure 13 presents the efficiency curves of five control strategies: PID, SMC, ASMC, FASMC, and MPC, enabling a comparative assessment of their energy conversion performance. Across all controllers, efficiency increases with rising output power. FASMC consistently achieves the highest efficiency, peaking at approximately 98.2%, due to its adaptive gains and fuzzy logic, which reduce switching losses and improve dynamic tracking. ASMC closely follows, with improved efficiency over SMC, thanks to its dynamic adjustment of control gains, reducing energy loss during transients. SMC shows moderate efficiency, higher than PID but lower than ASMC and FASMC, with fixed control gains limiting its adaptability to dynamic loads. PID exhibits the lowest efficiency, reaching about 95.0% at full load (500 W), due to its limited dynamic response and robustness. MPC offers strong and consistent performance, achieving up to 97.5% efficiency, with a relatively flat curve across all power levels, thanks to its predictive capabilities, though its computational complexity may pose implementation challenges. In summary, FASMC provides the highest efficiency, making it ideal for high-performance and high-power applications. MPC is a strong alternative with excellent consistency and noise resilience. ASMC and SMC offer reasonable efficiency improvements, while PID remains the least effective in energy conversion due to its limited adaptability and slower response.

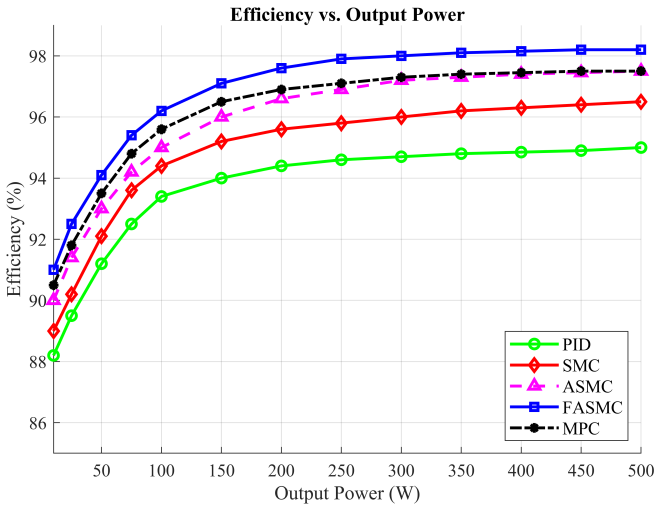

Figure 13. Efficiency comparison of five controllers

6. Conclusion

In this study, we have comprehensively evaluated and optimized various control strategies for half-bridge DC-DC buck converters. FASMC has emerged as the most effective approach, showcasing superior performance in rapid convergence, minimal error, and strong dynamic stability. The primary aim was to address significant challenges such as oscillation reduction, efficiency improvement, and tracking accuracy. The results provide a detailed comparison of the control strategies across various scenarios, highlighting the strengths and weaknesses of each technique. FASMC excels in managing initial condition disturbances, load disturbances, and noisy reference tracking, making it a robust solution for real-world applications. MPC is a close second, offering smooth and reliable performance but with a slight delay in convergence. ASMC and conventional SMC also provide robust and adaptive solutions, significantly improving upon the conventional PID control, which performs the weakest in all these scenarios. The integration of PSO for parameter optimization further enhances the performance of ASMC and FASMC, leading to better tracking accuracy, reduced control effort, and increased overall efficiency. This research underscores the advantages of advanced nonlinear and predictive control methods in addressing the challenges faced by half-bridge DC-DC buck converters, and highlights the potential of FASMC and PSO in achieving high performance and reliability.

6.1 *Possible directions for future work include*

1. Further optimization of the FASMC and ASMC controllers to enhance their performance under varying load conditions, input voltage fluctuations, and noisy environments.
2. Exploration of other advanced optimization techniques beyond PSO to refine the parameters of these controllers.
3. Implementation of the proposed control strategies in hardware to validate their performance in practical applications.
4. Comparison of the proposed controllers with other emerging control methods to gain new insights and potentially develop more innovative solutions.
5. Using hybrid optimization techniques that combine PSO with other algorithms, like GA or differential evolution, to explore a wider solution space and find more optimal control parameters.

Conflict of interest

The authors declare no competing financial interest.

References

[1] R. Islam, S. S. Rafin, and O. A. Mohammed, "Comprehensive review of power electronic converters in electric vehicle applications," *Forecasting*, vol. 5, no. 1, pp. 22-80, 2022.

[2] S. Harinaik, S. Sathyan, and N. M. Mary, "Design and analysis of modified series-parallel quasi-resonant half-bridge DC/DC converter for renewable energy applications," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 5, no. 3, pp. 1089-1099, 2023.

[3] D. Vinnikov, T. Jalakas, and M. Egorov, "Feasibility study of half-and full-bridge isolated DC/DC converters in high-voltage high-power applications," In Proc. International Power Electronics and Motion Control Conference, Poznan, Poland, Sep. 1-3, 2008, pp. 1257-1262.

[4] W. Phetphimoon and K. Bhumkittipich, "Modeling and simulation of bidirectional half bridge dc-dc converter," In Proc. International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), Chiang Mai, Thailand, Jun. 28, 2016, pp. 1-6.

[5] C. Bai, B. Han, and M. Kim, "A bidirectional switch based half-bridge series-resonant converter operating in DCM and CCM," In Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, Mar. 15, 2020, pp. 2109-2115.

[6] A. Amin, M. Shousha, A. Prodić, and B. Lynch, "A transformerless dual active half-bridge DC-DC converter for point-of-load power supplies," In Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, Sep. 20, 2015, pp. 133-140.

[7] S. S. Alharbi and M. Matin, "Experimental evaluation of medium-voltage cascode gallium nitride (GaN) devices for bidirectional DC-DC converters," *CES Transactions on Electrical Machines and Systems*, vol. 5, no. 3, pp. 232-248, 2021.

[8] C. Buccella, C. Cecati, H. Latafat, and K. Razi, "Digital control of a half-bridge LLC resonant converter," In Proc. International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, Serbia, Sep. 4, 2012, pp. LS6a-4.

[9] O. Tahmaz and A. B. Yıldız, "Efficient modeling technique for analysis of the half bridge DC-DC converter," In Proc. European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, Sep. 6-10, 2021, pp. P-1.

[10] M. A. Awadallah, E. H. Bayoumi, and H. M. Soliman, "Adaptive deadbeat controllers for brushless DC drives using PSO and ANFIS techniques," *Journal of Electrical Engineering*, vol. 60, no. 1, pp. 3-11, 2009.

[11] H. Abderrezek and M. N. Harmas, "PSO based adaptive terminal sliding mode controllers for a DC-DC converter," *International Journal of Computer Theory and Engineering*, vol. 6, no. 4, p. 302, 2014.

[12] M. A. Abido, "Optimal design of power-system stabilizers using particle swarm optimization," *IEEE Transactions on Energy Conversion*, vol. 17, no. 3, pp. 406-413, 2002.

[13] M. R. AlRashidi, M. F. AlHajri, A. K. Al-Othman, and K. M. El-Naggar, "Particle swarm optimization and its applications in power systems," in *Computational Intelligence in Power Engineering*, Berlin, Germany: Springer Berlin Heidelberg, 2010, pp. 295-324.

[14] J. D. Cham, F. L. Koffi, A. T. Boum, and A. Harrison, "Robust adaptive integral sliding mode control of a half-bridge bidirectional DC-DC converter," *International Journal of Electrical and Computer Engineering*, vol. 15, no. 1, pp. 2397-2408, 2025.

[15] A. Domyshev, E. Chistyakova, A. Dreglea, D. Sidorov, and F. Liu, "DC-DC converters optimization in case of large variation in the load," In Proc. Chinese Control Conference (CCC), Tianjin, China, Jul. 28, 2024, pp. 4246-4250.

[16] J. Ramos-Hernanz, J. M. Lopez-Guede, O. Barambones, E. Zulueta, and U. Fernandez-Gamiz, "Novel control algorithm for MPPT with boost converters in photovoltaic systems," *International Journal of Hydrogen Energy*, vol. 42, no. 28, pp. 17831-17855, 2017.

[17] B. N. Abramovich, D. A. Ustinov, and W. J. Abdallah, "Modified proportional integral controller for single ended primary inductance converter," *International Journal of Power Electronics and Drive Systems*, vol. 13, no. 2, pp. 1007-1017, 2022.

[18] M. H. Ashfaq, A. Jeyraj, L. Selvaraj, and N. Abd Rahim, "Control strategies for bidirectional DC-DC converters: an overview," In Proc. IOP Conference Series: Materials Science and Engineering, Chennai, India, Mar. 1, 2021, vol. 1127, no. 1, p. 012031.

[19] D. M. Abraham, "PWM-based sliding mode current controller for bidirectional DC-DC converters in electric vehicles," In Proc. International Conference on Power, Instrumentation, Control and Computing (PICC), Thrissur, India, Dec. 17, 2020, pp. 1-6.
[20] K. H. Ang, G. Chong, and Y. Li, "PID control system analysis, design, and technology," *IEEE Transactions on Control Systems Technology*, vol. 13, no. 4, pp. 559-576, 2005.
[21] A. Debnath, T. O. Olowu, S. Roy, I. Parvez, and A. Sarwat, "Particle swarm optimization-based PID controller design for DC-DC buck converter," In Proc. North American Power Symposium (NAPS), College Station, TX, USA, Nov. 14, 2021, pp. 1-6.
[22] M. Eldoromi, A. A. Birjandi, and N. M. Dehkordi, "Anti-windup control strategy for interlinking converters in hybrid AC/DC microgrids with EV charging stations," *Electric Power Systems Research*, vol. 247, p. 111800, Oct. 2025.
[23] J. B. Rawlings and M. J. Risbeck, "Model predictive control with discrete actuators: Theory and application," *Automatica*, vol. 78, pp. 258-265, 2017.
[24] S. H. Zak, "An introduction to model-based predictive control (MPC)," Purdue University, West Lafayette, IN, USA, Tech. Rep., 2017. [Online]. Available: https://engineering.purdue.edu/~zak/ECE680/MPC_handout.pdf. [Accessed Jan. 15, 2025].
[25] F. J. Padilha and M. D. Bellar, "Modeling and control of the half-bridge voltage-doubler boost converter," In Proc. IEEE International Symposium on Industrial Electronics, Rio de Janeiro, Brazil, Jun. 9, 2003, vol. 2, pp. 741-745.
[26] V. Utkin, "Sliding mode control of DC/DC converters," *Journal of the Franklin Institute*, vol. 350, no. 8, pp. 2146-2165, 2013.
[27] A. Yazidi and F. Betin, "Robust sliding mode control for electrical drives," *International Journal of Electrical Engineering and Technology*, vol. 12, no. 12, pp. 26-36, 2021.
[28] K. B. Saad, A. Sahbani, M. Benrejeb, and A. Bartoszewicz, "Sliding mode control and fuzzy sliding mode control for DC-DC converters," *Sliding Mode Control*, pp. 1-24, 2011, https://doi.org/10.5772/15151.
[29] S. M. RakhtAla, M. Yasoubi, and H. HosseinNia, "Design of second order sliding mode and sliding mode algorithms: a practical insight to DC-DC buck converter," *IEEE/CAA Journal of Automatica Sinica*, vol. 4, no. 3, pp. 483-497, 2017.
[30] J. D. Cham, F. L. Koffi, A. T. Boum, and A. Harrison, "Robust adaptive sliding mode control of a bidirectional DC-DC converter feeding a resistive and CPL based on PSO," *International Journal of Power Electronics and Drive Systems*, vol. 15, no. 4, pp. 2397-2408, 2024.
[31] Y. Yang, Y. Wang, W. Zhang, Z. Li, and R. Liang, "Design of adaptive fuzzy sliding-mode control for high-performance islanded inverter in micro-grid," *Energies*, vol. 15, no. 23, p. 9154, 2022.
[32] X. Dominguez, O. Camacho, P. Leica, and A. Rosales, "A fixed-frequency sliding-mode control in a cascade scheme for the half-bridge bidirectional DC-DC converter," In Proc. IEEE Ecuador Technical Chapters Meeting (ETCM), Guayaquil, Ecuador, Oct. 12, 2016, pp. 1-6.
[33] G. Balta, Ç. Hisar, and N. Altin, "Artificial intelligence based switching frequency regulation with fast terminal sliding mode control for DC-DC step-down converters," *Expert Systems with Applications*, vol. 228, p. 120331, 2023.
[34] G. Balta, N. Güler, and N. Altin, "Global fast terminal sliding mode control with fixed switching frequency for voltage control of DC-DC buck converters," *ISA Transactions*, vol. 143, pp. 582-595, 2023.
[35] J. D. Cham, F. L. Koffi, A. T. Boum, A. Harrison, P. M. Zemgue, and N. H. Alombah, "Accurate and optimal control of a bidirectional DC-DC converter: A robust adaptive approach enhanced by particle swarm optimization," *e-Prime-Advances in Electrical Engineering, Electronics and Energy*, vol. 11, p. 100899, 2025.
[36] Y. Nettari and M. N. Harmas, "Genetic algorithm based adaptive fuzzy terminal synergetic DC-DC converter control," In Proc. International Conference on Control, Engineering and Information Technology (CEIT), Tlemcen, Algeria, May. 25, 2015, pp. 1-7.
[37] M. M. Nishat, F. Faisal, M. A. Hoque, A. J. Evan, M. M. Rahaman, M. S. Sifat, and H. M. Fazle Rabbi, "Stability analysis and optimization of simulated annealing (SA) algorithm based PID controller for DC-DC SEPIC converter," *International Journal of Computer Science and Network Security*, vol. 19, no. 9, pp. 1-8, 2019.
[38] B. Rani Jose, M. Chacko, and H. Kuttomparambil, "Efficiency enhancement in DC-DC boost converters using WBG switches through PSO optimized FOPID controller for solar systems," *Advanced Control for Applications: Engineering and Industrial Systems*, vol. 7, no. 2, p. e70016, 2025.
[39] P. Veeramanikandan, G. N. Veena, R. Giri Prasad, and E. Muniyandy, "Optimizing DC-DC converter topologies for enhanced efficiency in hybrid renewable energy systems using hybrid techniques," *Wind Engineering*, pp. 1-15, 2025.

[40] F. Bagheri, N. Guler, H. Komurcugil, and S. Bayhan, "An adaptive sliding mode control for a dual active bridge converter with extended phase shift modulation," *IEEE Access*, vol. 11, pp. 91260-91274, 2023.

[41] M. Leso, J. Zilkova, M. Pastor, and J. Dudrik, "Fuzzy logic control of soft-switching DC-DC converter," *Elektronika ir Elektrotechnika*, vol. 22, no. 5, pp. 3-7, 2016.

[42] J. B. Fermeiro, J. A. Pombo, M. R. Calado, and S. J. Mariano, "Evaluation of a particle swarm optimization controller for DC-DC boost converters," In Proc. International Conference on Compatibility and Power Electronics (CPE), Costa da Caparica, Portugal, Jun. 24, 2015, pp. 179-184.

[43] B. M. Sarif, D. A. Kumar, and M. V. Rao, "Comparison study of PID controller tuning using classical analytical methods," *International Journal of Applied Engineering Research*, vol. 13, no. 8, pp. 5618-5625, 2018.

[44] L. Wu, J. Liu, S. Vazquez, and S. K. Mazumder, "Sliding mode control in power converters and drives: A review," *IEEE/CAA Journal of Automatica Sinica*, vol. 9, no. 3, pp. 392-406, 2021.

[45] N. Kuyvenhoven, "PID tuning methods an automatic PID tuning study with Mathcad," Calvin College, Grand Rapids, MI, USA, Tech. Rep., Dec. 2002. [Online]. Available: https://www.calvin.edu/~nkuyvenh/Research/PIDTuningStudy.pdf. [Accessed Jan. 15, 2025].

[46] O. Ibrahim, N. Yahaya, and N. Saad, "Design and implementation challenges of digital controlled DC-DC converters," *Journal of Mechanical Continua and Mathematical Sciences*, vol. 13, no. 3, pp. 1-15, 2018.

[47] M. Safdari, M. R. Alizadeh Pahlavani, and A. Dehestani Kolagar, "Model predictive voltage balance control of single-phase half-bridge active front end rectifier," *International Journal of Industrial Electronics Control and Optimization*, vol. 6, no. 2, pp. 81-88, 2023.

[48] X. Chen, S. Kawai, and T. Nguyen-Van, "Model predictive control for stand-alone half-bridge inverter," In Proc. IEEE Global Conference on Consumer Electronics (GCCE), Nara, Japan, Oct. 10, 2023, pp. 1183-1187.

[49] H. Ben Mansour, K. Dehri, and A. S. Nouri, "Comparison between predictive sliding mode control and sliding mode control with predictive sliding function," in *Recent Advances in Electrical Engineering and Control Applications*, Cham, Switzerland: Springer International Publishing, 2016, pp. 80-97.

[50] H. Guldemir, "Study of sliding mode control of DC-DC buck converter," *Energy and Power Engineering*, vol. 3, no. 4, pp. 401-406, 2011.

[51] J. R. Ortiz-Castrillón, S. D. Saldarriaga-Zuluaga, N. Muñoz-Galeano, J. M. López-Lezama, S. Benavides-Córdoba, and J. B. Cano-Quintero, "Optimal sliding-mode control of semi-bridgeless boost converters considering power factor corrections," *Energies*, vol. 16, no. 17, p. 6282, 2023.

[52] J. D. Cham, F. L. Koffi, A. T. Boum, and A. Harrison, "Robust adaptive integral sliding mode control of a half-bridge bidirectional DC-DC converter," *International Journal of Electrical and Computer Engineering*, vol. 15, no. 1, pp. 2397-2408, 2025.

[53] C. L. Chen, "Many-objective adaptive fuzzy with sliding mode control for a class of switching power converters using global optimization," *IEEE Access*, vol. 10, pp. 10317-10332, 2022.

[54] A. G. Saravanan and M. Rajaram, "Fuzzy controller for dynamic performance improvement of a half-bridge isolated DC-DC converter," *Neurocomputing*, vol. 140, pp. 283-290, 2014.

[55] L. Guo, J. Y. Hung, and R. M. Nelms, "Evaluation of DSP-based PID and fuzzy controllers for DC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2237-2248, 2009.

[56] R. Pramanik and B. B. Pati, "Modelling and control of a non-isolated half-bridge bidirectional DC-DC converter with an energy management topology applicable with EV/HEV," *Journal of King Saud University-Engineering Sciences*, vol. 35, no. 2, pp. 116-122, 2023.

[57] T. J. Liang and J. H. Lee, "Novel high-conversion-ratio high-efficiency isolated bidirectional DC-DC converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4492-4503, 2014.

[58] F. Jarraya, A. Khan, A. Gastli, L. Ben-Brahim, and R. Hamila, "Design considerations, modelling, and control of dual-active full bridge for electric vehicles charging applications," *The Journal of Engineering*, vol. 2019, no. 12, pp. 8439-8447, 2019.

[59] Z. Guo, X. Zheng, C. Jin, Y. Fan, M. Cai, J. Zhou, W. Dong, Q. Luo, and B. Shen, "A new Fe-based nanocrystalline soft magnetic composites with ultra-low core loss and superior DC-bias permeability up to megahertz-frequency," *Materials Today Nano*, vol. 30, p. 100621, 2025.

[60] Q. Ullah, T. D. Busarello, D. I. Brandao, and M. G. Simões, "Design and performance evaluation of SMC-based DC-DC converters for microgrid applications," *Energies*, vol. 16, no. 10, p. 4212, 2023.

[61] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Springer Science & Business Media, 2007.
[62] I. Bouchriha, A. BenGhanem, and K. Nour, "Optimization of the sliding mode control (SMC) with the particle swarm optimization (PSO) algorithm for photovoltaic systems based on MPPT," *Advances in Science, Technology and Engineering Systems Journal*, vol. 7, pp. 100-106, 2022.
[63] S. C. Tan, Y. M. Lai, C. K. Tse, and M. K. Cheung, "An adaptive sliding mode controller for buck converter in continuous conduction mode," In Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, Feb. 22-26, 2004.
[64] X. Zhang, Y. Zhao, H. Jiang, and M. Wei, "Design of integral sliding mode control and fuzzy adaptive PI control for voltage stability in DC microgrid," *Frontiers in Energy Research*, vol. 11, p. 1278305, 2023.
[65] S. Rajendran, A. M. Kumar, and V. A. Selvi, "Particle swarm optimization tuned hybrid sliding mode controller based static synchronous compensator with LCL filter for power quality improvement," *Sustainable Energy Technologies and Assessments*, vol. 53, p. 102653, 2022.