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Research Article

Design Techniques for Ultra-Low Power Ring Oscillators: A Comparative Survey

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Abstract: The growing need for ultra-low power timing circuits in energy-harvesting circuitry, Internet of Things nodes, and bio-medical implants has spurred Ring Oscillator (RO) design innovation. ROs are largely selected because of digital compatibility, smaller size, and ease of integration. However, conventional designs suffer from severe challenges to power efficiency as well as resilience to environment and process variation. The present paper is a survey of the optimum techniques evolved to achieve RO optimization at ultra-low power. Six general classes of design methods are introduced: sub-threshold operation, current-starved inverters, body biasing methods, capacitive loading, digital calibration, and process-aware optimizations. Each approach is compared in terms of power consumption, frequency range, area overhead, and robustness, with exhaustive comparisons drawn from recent literature. Different application domains from energy-constrained sensors to digitally intensive SoCs are addressed. The paper further identifies issues such as frequency instability, variability between process corners, and scalability in late nodes. Some potential areas of future work are suggested in the context of variation-aware design, adaptive calibration, and technology-aware integration. The review serves as a guideline in selecting and designing low-power oscillator architectures specific to the needs of some applications.

Keywords: body biasing, current-starved inverter, digital calibration, energy-harvesting, Fully Depleted Silicon-on-Insulator (FD-SOI), Internet of Things (IoT), process variation, Ring Oscillator (RO), ultra-low power design

1. Introduction

The rapid growth of battery-assisted and energy-harvesting electronic devices such as wireless sensor networks, biomedical implants, and Internet of Things (IoT) devices has created an excessive need for ultra-low power circuit components [1, 2]. Among these components, oscillators are vital in supplying clock signals, enabling timing references, and supporting various analog and digital operations. Out of numerous oscillator architectures, Ring Oscillators (ROs) have garnered significant attention due to their simple structure, easy integration, and scalability with Complementary Metal Oxide Semiconductor (CMOS) technology.

While traditional ROs are valued for their compact size and high tunability, their relatively large power consumption and temperature and process sensitivity are limitations in ultra-low power environments. Therefore, much research has focused on creating ways to reduce power consumption in Ring Oscillators without necessarily compromising performance metrics such as frequency stability, startup time, and area efficiency.

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A number of low-power techniques have been suggested over the past two decades, including sub-threshold operation, current-starved inverter design, body biasing, and digital calibration circuits. Each technique offers other trade-offs in terms of power, area, and insensitivity to variations. Additionally, emerging technologies such as FD-SOI and FinFET [3] have enabled further advancements in energy efficiency[4] and frequency control[5].

The paper follows the following organization: Section 2 outlines the fundamental concepts and performance parameters of Ring Oscillators. Section 3 provides an overview of six prominent ultra-low power design methods based on supporting literature and diagrams. Section 4 offers comparative analysis in terms of power, frequency, and process hardness. Section 5 outlines contemporary challenges and directions for future research, and Section 6 concludes with key takeaways and recommendations on application-specific design choices.

2. Ring Oscillator fundamentals

The Ring Oscillator (RO) is a circuit consisting of an odd number of NOT gates (inverters) in a loop, whose output alternates between two voltage levels, true and false. The NOT gates are connected in a chain, and the output of the last inverter is fed back to the first one, such that the signal loops around the chain and oscillates. Ring Oscillators are widely used in clock generation [6], temperature sensing [7], and as sources of entropy in Physically Unclonable Functions (PUFs) [8] because they are small, all-digital, and easily integrable [9].

2.1 *Operating principle*

The minimum design of an RO includes an odd number (usually 3, 5, or 7) of inverters, every one of which contributes a delay. As a signal moves through the chain and returns to the input, it is inverted, causing sustained oscillation [10]. The frequency of oscillation is given by:

$$fosc = \frac{1}{2Ntd}$$

where:

N is the number of inverter stages

td is the propagation delay of each inverter

2.2 *Key performance metrics*

The following parameters describe the performance of a Ring Oscillator:

Power consumption: Dynamic switching and leakage controlled, most critical in low-power applications.

Frequency stability: Determined by supply voltage, temperature, and process variations.

Phase noise / jitter: Most critical in communications and timing-sensitive applications.

Startup time: Time for the oscillator to begin stable oscillation.

Area: Determined by the number of stages and complexity of delay elements.

Temperature sensitivity: ROs are temperature-dependent inherently due to mobility and threshold variations.

2.3 *Design trade-offs*

Ring Oscillators typically involve several trade-offs that need to be optimized:

Power-frequency trade-off: Lowering supply voltage lowers power but also frequency and raises delay.

Area-stability trade-off: Techniques like adding control or calibration circuitry increase robustness at the cost of additional silicon area.

Noise-power trade-off: Aggressive Low-power techniques can further reduce jitter and phase noise.

3. Ultra-low power techniques classification

A number of techniques have been proposed to reduce power consumption in Ring Oscillator circuits over time. These methods are broadly categorized as design-level methods (e.g., biasing, transistor sizing), circuit-level methods (e.g., current-starved architectures), and system-level methods (e.g., digital calibration and temperature compensation). Every technique offers trade-offs involving power, frequency, area, and robustness. This section presents a classified overview of widely utilized techniques.

3.1 *Near-threshold and sub-threshold operation*

Sub-threshold operation is a well-established technique for achieving ultra-low power consumption in CMOS Ring Oscillators. By operating transistors below their threshold voltage (V_{th}), the circuit exploits the exponentially small sub-threshold current, leading to drastically reduced dynamic and leakage power. However, this also results in increased propagation delay and reduced frequency, making such oscillators more suitable for low-frequency timing applications.

A fascinating implementation demonstrates a Ring Oscillator design optimized for oscillation in the deep sub-threshold region at the minimum supply voltage of 0.25 V [11]. The novel topology replaces the conventional push–pull inverter stages (Figure 1) with a common-source inverter structure (Figure 2), combined with a supply-independent biasing circuit. The design allows the circuit to have a fixed frequency and current for a wide supply voltage range (0.25-1.25 V). The circuit is capable of reducing power consumption to as low as 2.9 pW at an output frequency of around 2 Hz, making it extremely suitable for ultra-low-power and energy-harvesting applications.

The use of a reference voltage generator in the biasing circuit gives the circuit the stability against supply fluctuations, which is otherwise the weak area in sub-threshold designs. As with the majority of sub-threshold oscillators, the design is highly sensitive to process and temperature variations, and due to its low frequency, it is suitable for utilization only in small timing domains.

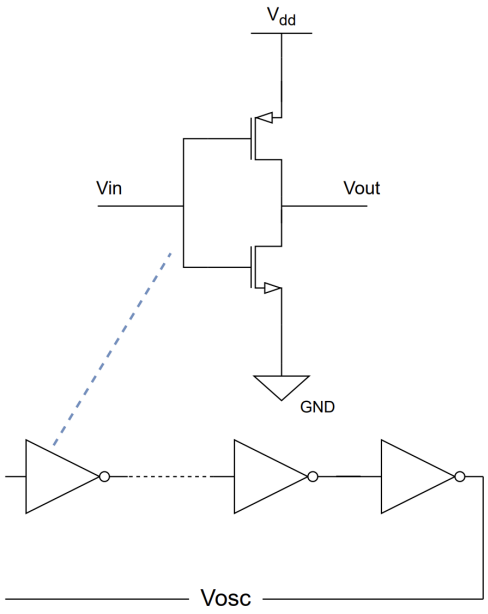

Figure 1. Conventional Ring Oscillator with push–pull inverter used as a construction unit [11]

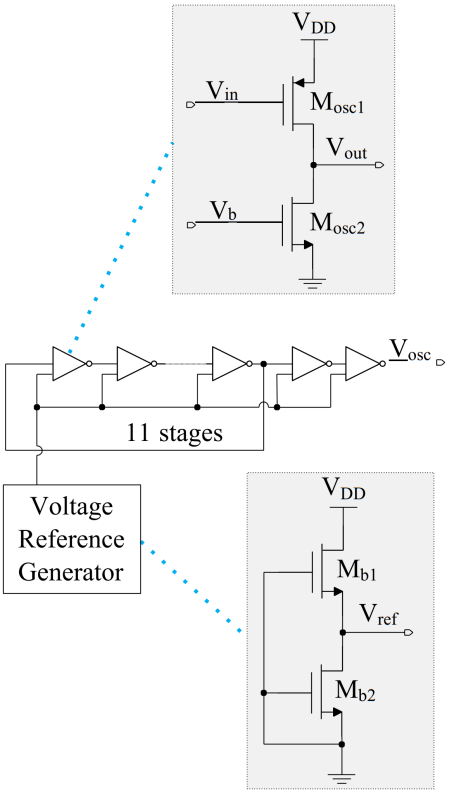

Figure 2. Ultra-low-power CMOS Ring Oscillator using common source inverter stage and reference voltage circuit [11]

3.2 *Current-starved inverter topology*

Current-Starved Ring Oscillator (CSRO) is a popular architecture for programmable frequency and ultra-low power operation in contemporary CMOS designs. In CSRO, current to the inverter stages is starved by control transistors acting as current sources and thus effectively "starve" the inverter. This approach allows accurate delay and frequency control with reduced overall power consumption.

Several recent designs have employed the CSRO topology to achieve power-performance trade-offs:

A CMOS temperature sensor was designed using a current-starved Ring Oscillator topology in the sub-threshold region at a supply voltage of as low as 0.2 V [12]. The sensor employed a PTAT current source starving the oscillator and generating an output frequency of 50 MHz when the power consumed was only 3.75 pW. A Bit-Weighted Current Mirror (BWCM) was employed for process variation compensation and for increasing current stability. The structure of CSRO, as illustrated in Figure 3, comprises an odd number of inverters in a loop, with each inverter supplied with limited current by P-channel Metal Oxide Semiconductor (PMOS) and N-channel Metal Oxide Semiconductor (NMOS) current sources. Special care was taken while designing the current mirrors and source transistors to keep leakage minimized despite process and temperature variations.

In addition to this, the design of a current-starved Voltage Controlled Oscillator (VCO) for low power applications with 32 nm technology was studied in [13]. They demonstrated that the use of Dynamic Threshold MOSFET (DTMOS) configurations for the current source transistors enhanced the frequency stability considerably over temperature variations, relative to traditional VCOs. As evidenced through their performance graphs (Figures 4 and 5), the CSRO with DTMOS interface achieved a 48% speed boost through only an 18.9% increase in power at V_{DD} = 0.4 V.

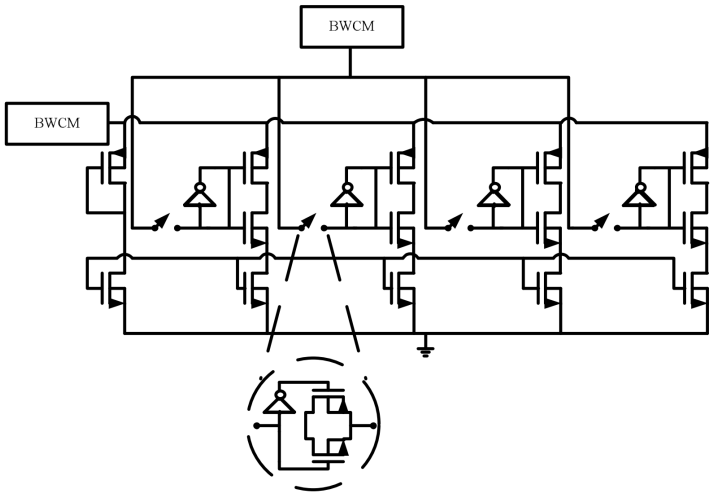

Figure 3. Current Starved Ring Oscillator (CSRO) [12]

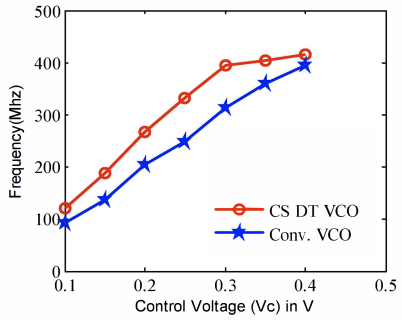

Figure 4. Frequency as a function of Control Voltage at V_{DD} = 0.4 V [13]

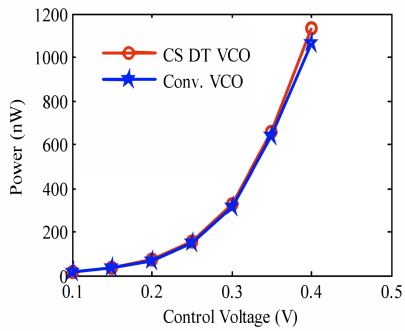

Figure 5. Power as a function of Control Voltage at V_{DD} = 0.4V [13]

These enhancements point to the flexibility of the current-starved topology, not just in reducing static and dynamic power but also in enhancing supply and environmental variation robustness. CSRO designs are however control current calibration sensitive, and the achievable frequency is bounded by the maximum allowable current through the biasing network.

3.3 *Body biasing methods*

Body biasing is a strong technique applied in CMOS and FD-SOI technology for dynamically setting transistors' threshold voltage (Vth) dynamically. By controlling the Body-to-Source Voltage (VBS), designers can either enhance speed (forward body biasing) or reduce leakage power (reverse body biasing), making the technique highly beneficial for ultra-low power and energy-harvesting applications.

In Forward Body Biasing (FBB), NMOS devices are given a negative bias and PMOS devices are given a positive bias, which in effect reduces Vth and drive current. This enhances the speed of switching but at the cost of higher leakage. This is reversed in Reverse Body Biasing (RBB), which increases Vth and therefore reduces leakage currents and total power dissipation but at the cost of speed.

A significant improvement over traditional body biasing methods, presented a self-cascoded body biasing method for sub-threshold Ring Oscillators [14]. The proposed design is aimed at self-powered IoT devices and provides better low-power performance than the conventional FBB and RBB schemes.

In their architecture, auxiliary transistors are employed to establish dynamic bulk voltages for NMOS and PMOS devices (Figure 6). The dynamic biasing raises or lowers the threshold voltages under operation without using an external bias generator. From their small-signal model (Figure 7), this structure is shown to improve transistor drive current, enhance frequency stability, and lower subthreshold leakage.

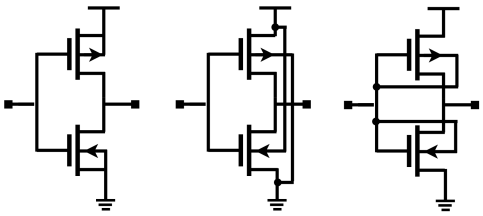

Figure 6. (from left to right): (a) Standard body bias CMOS (b) Forward Body Bias (FBB) CMOS (c) Dynamic Threshold (DT) CMOS [14]

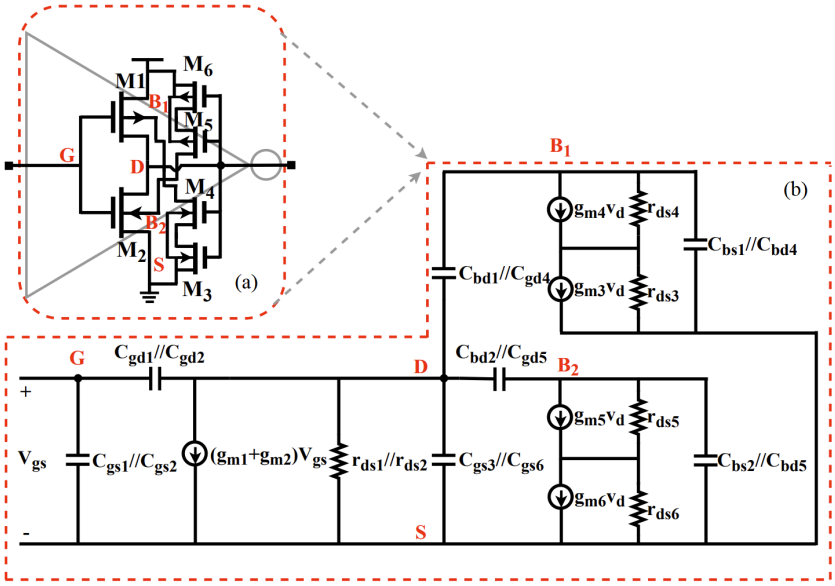

Figure 7. (a) Inverter using self cascaded body biasing (b) Corresponding simplified small-signal equivalent model [14]

Post-layout simulation yields that the design proposed here operates at minimum supply voltage of 270 mV with a frequency of oscillation of 2.65 MHz and a power of only 58.9 nW (Table 1) [14]. Comparing with traditional FBB, DBB (Dynamic Body Biasing), and RBB, the lowest power consumption and variation in frequency against process and temperature variations is that of the self-cascoded method.

Table 1. RO with various bulk biasing techniques [14] (FBB*: Forward Body Biasing with single transistor)

Design	Minimum supply voltage (mV)	Power (nW)	Frequency (MHz)	Area (mm^2)
Proposed	270	58.9	2.65	0.00058
FBB*	280	69.1	2.6	0.00055
DBB	310	190	2.51	0.00038
FBB	295	73.72	2.59	0.00038
RBB	325	86.5	2.49	0.00038

Transient simulation (Figure 8) illustrates that most of the potentials of NMOS and PMOS devices swing dynamically above the supply and below the ground rails, respectively, which is a significant contributor to the enhanced drive current and robustness.

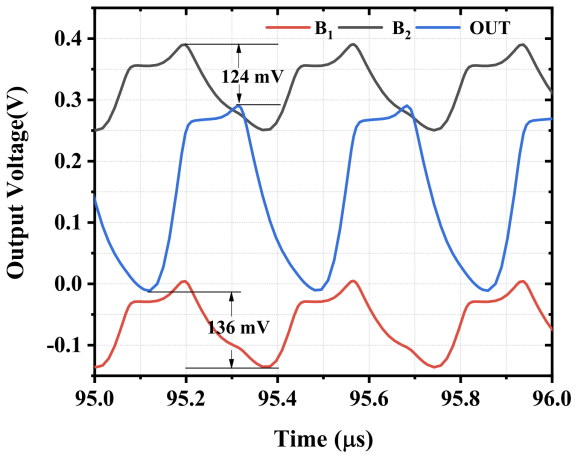

Figure 8. Transient response of the output voltage and bulk terminal voltages at 270 mV supply voltages [14]

Besides, temperature variation performance illustrates that the designed self-cascoded Ring Oscillator achieves more stable operation compared to traditional body-biasing methods (Table 2) [14].

Table 2. Corner and temperature simulation results of the proposed RO at 270 mV [14]

Parameter	Corner	Temperature (°C)		
		0	27	75
Frequency (MHz)	SS	0.102	0.47	2.08
	TT	0.932	2.61	7.89
	FF	4	9.1	24.3
Power (nW)	SS	2.43	10.61	47.36
	TT	20.65	58.9	186.1
	FF	90.42	208.5	585.5

3.4 *Capacitive loading and delay control*

Capacitive loading is an easy way to frequency tuning of Ring Oscillators. By adjusting the effective load capacitance at the inverter outputs, the per-stage propagation delay is modified, hence the frequency can be tuned. The method is attractive due to its ease of implementation and integration with digital control circuits.

A design of Digitally Controlled Ring Oscillator (DCRO) was presented with PMOS-based MOS varactors to control the capacitive load at each stage (Figure 9). Digital control bits selectively enable various varactors, allowing discrete frequency steps with minimal dynamic power variation. The design had a tuning range of 0.890 GHz to 0.916 GHz with load capacitance control and an additional extension to 1.222 GHz using supply voltage scaling. Minimum power consumption of 0.269 mW was observed at 1.8 V supply [15].

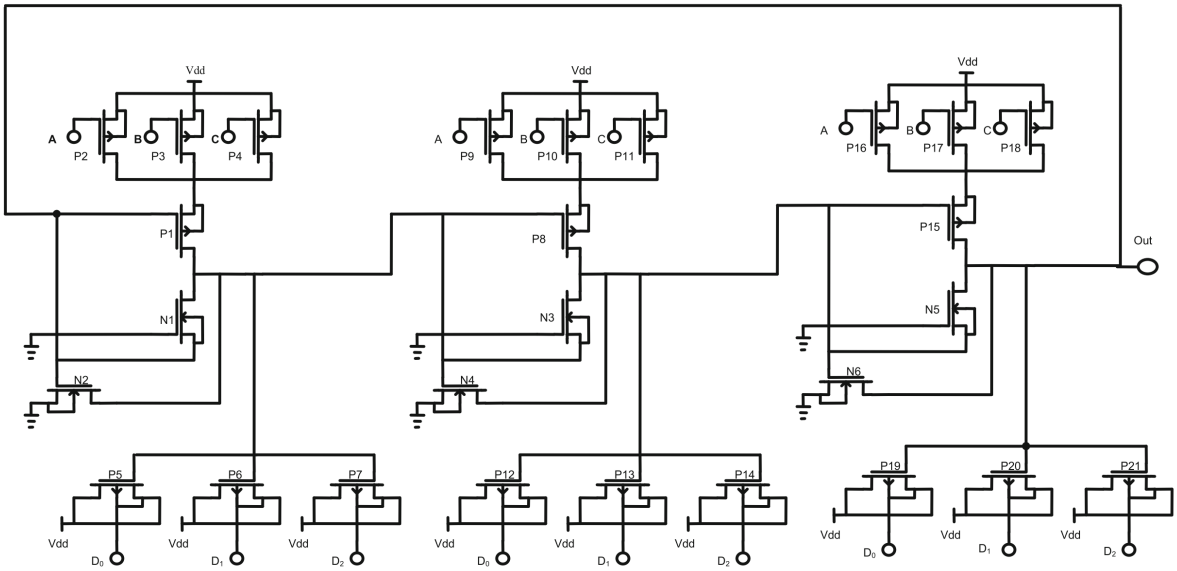

Figure 9. 3-stage ring DCRO [15]

While capacitive load control provides high frequency resolution and ease of digital programmability, it introduces parasitic capacitances and reduces phase noise unless it is properly designed. Compared to other ultra-low-power techniques such as body biasing and sub-threshold operation, capacitive tuning techniques possess less drastic power reduction and frequency stability enhancement but remain beneficial in applications requiring small and digitally programmable oscillators.

Recent advancements have explored capacitor-based delay control to facilitate fine-grained frequency tuning in ultra-low power Ring Oscillators. Involving a Complementary Drain Capacitance (CDC), as shown in a study which proposed a Controlled Ring Oscillator (CRO-CDC) topology suitable for UWB [16]. By incorporating a digitally controlled capacitance structure with PMOS and NMOS drain terminals, their design is capable of tunability without significantly increasing circuit complexity or power consumption. The study contrasts various implementations including basic negator, NAND, and NOR-based delay cells, and shows that the CRO-CDC delivers output frequency ranges of up to 5.619 GHz at minimum power consumption of 0.595mW, while achieving acceptable phase noise and FoM values. This approach illustrates how careful control of capacitive loading can lead to low-power, high-speed designs suitable for digital control and scalable CMOS processes.

3.5 *Digital calibration and feedback techniques*

Digital calibration techniques have also become essential in Ring Oscillator (RO) design to resist performance fluctuation due to Process, Voltage, and Temperature (PVT) variations. With the incorporation of digital feedback loops

and trimming networks, designers are able to fine-tune the oscillator parameters following fabrication to enhance frequency stability without requiring external crystals or analog fine-tuning circuits.

A digitally calibrated low-power Ring Oscillator was proposed in a study that included a closed-loop calibration loop made up of a programmable delay block, a frequency comparator, and a control logic block [17]. As illustrated in Figure 10, the oscillator's output is compared with a reference clock, and the calibration logic always tunes the capacitive load setting of all the delay stages so that the output frequency is set to the target value. The delay stages themselves, as depicted in Figure 11, consist of digitally adjustable capacitive components that adjust the effective delay per stage according to the control inputs.

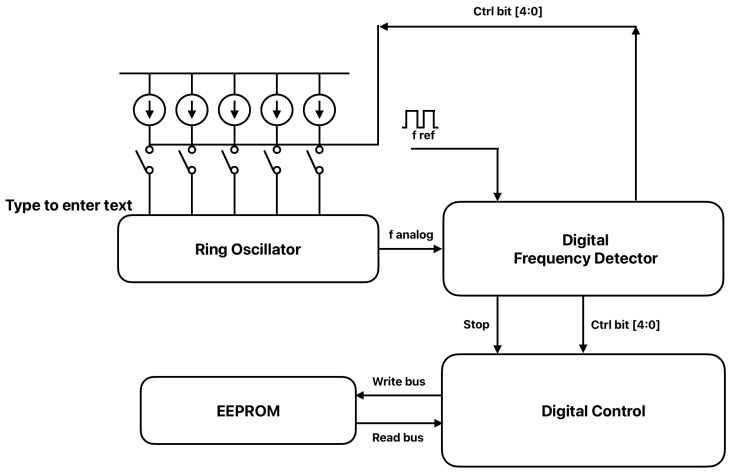

Figure 10. The structure of the top circuit [17]

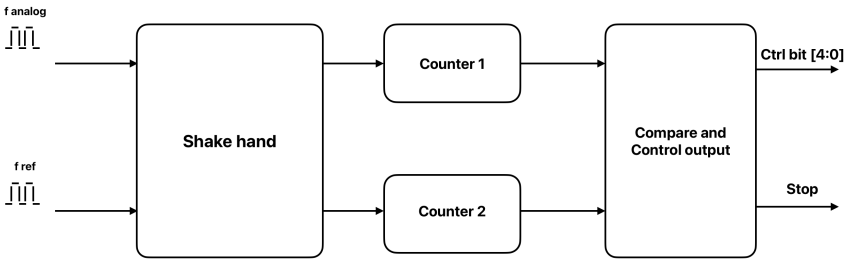

Figure 11. The structure of the digital module [17]

The digitally calibrated RO, developed in 65 nm CMOS technology, operates at a nominal supply voltage of 1.2 V. It possesses programmable frequency tuning from approximately 100 MHz to 250 MHz with minimal power consumption of 35 μ W at highest frequency. The digital calibration reduces frequency variation over process corners by more than 50%, demonstrating the effectiveness of the calibration approach in preventing fabrication-caused variability.

In the recent times, digital calibration methods become extremely crucial in delivering frequency accuracy and reliability, particularly when integrating into clock generation and frequency synthesizer systems. An important contribution in this area proposed a frequency synthesizer that employs an automatically frequency-calibrated digitally controlled Ring Oscillator [18]. The architecture demonstrates immunity to early-phase errors and environmental ambiguity by employing

a dual-mode feedback loop, a fast digital calibration loop for coarse correction and a fine analog Phase-Locked Loop (PLL) for steady-state lock.

In addition to the AFC mechanism, the article introduces a Phase-Noise Enhanced Ring Oscillator (PNERO), which replaces conventional delay cells with pseudo-differential buffer stages. This improvement not only minimizes power consumption but also significantly improves phase noise performance, a significant constraint in the traditional RO-based synthesizers. Startup insensitivity, frequency accuracy at PVT corners, and competitive Figure-of-Merit (FoM) values for IoT and wireless applications are ensured by the calibration architecture. These results emphasize the increasing practicality of digitally calibrated feedback-aided ROs for applications that demand low jitter and consistent frequency characteristics within power limitations.

Compared to analog trimming methods, digital calibration offers greater programmability, reliability, and integration flexibility, especially in scaled technologies where analog variability is larger. Although it incurs a small area overhead due to the additional calibration logic, the benefits in frequency accuracy and flexibility make it an attractive solution for ultra-low-power clock generation, wireless transceivers, and system-on-chip timing circuits.

3.6 *Process-aware and technology-optimized designs*

The development of manufacturing technologies such as Fully Depleted Silicon-on-Insulator (FD-SOI) and FinFET in 22 nm and 14 nm nodes has introduced new opportunities for Ring Oscillator (RO) performance enhancement with stringent power, area, and reliability constraints. Process-specific properties such as body biasing in FD-SOI and improved short-channel control in FinFETs are increasingly being employed to design ultra-low-power and highly stable oscillators.

The prospects of FD-SOI technology through proposing a nano-scaled Ring Oscillator in Dual-Metal Insulated Gate (DMIG) FD-SOI MOSFETs was explored in [19]. The DMIG FD-SOI structure, as illustrated in Figure 12, involves dual metal gates separated by a high-k dielectric layer (HfO_2) to offer improved control over short-channel effects and leakage suppression. The DMIG FD-SOI structure had an excellent Ion/Ioff switching ratio of 10^12, low subthreshold slope close to 62 mV/decade, and oscillation frequency of 84.18 GHz at channel length of 50 nm, hence it is highly suitable for IC dense applications.

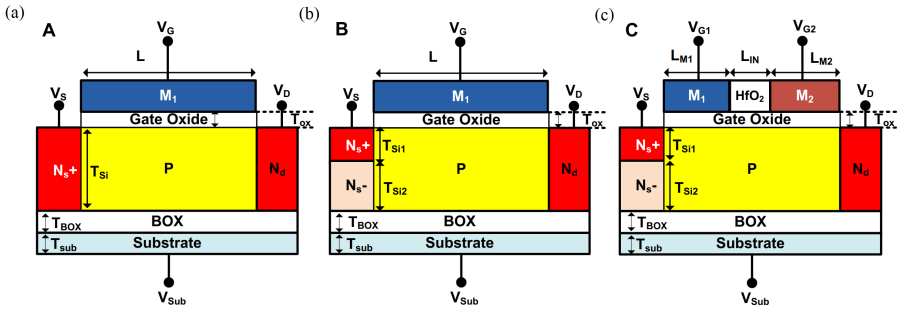

Figure 12. Devices under consideration: (a) conventional FD-SOI MOSFET, (b) referenced FD-SOI MOSFET [15], (c) proposed DMIG Source Engineered FD-SOI MOSFET [19]

The simulated fabricated CMOS inverter and Ring Oscillator circuits with TCAD tools revealed lower parasitic capacitances and improved gate control, as observed from the better surface potential profile and flat conduction current density plots (Figure 13). Transient analysis also exhibited negligible propagation delays, allowing for high-frequency operation with negligible leakage penalties.

Together with these accomplishments, a study reported an ultra-low-power duty cycling oscillator in 22 nm FD-SOI technology [20]. With independent back-gate biasing capabilities, their integration achieved frequency tuning between 7 kHz and 62 kHz with total DC power consumption of less than 9 nW at supply voltage of 0.5 V. The oscillator topology presented in Figure 14 utilizes long-channel devices with digitally tunable resistive and capacitive loads to enable coarse and fine frequency tuning through back-gate voltage settings.

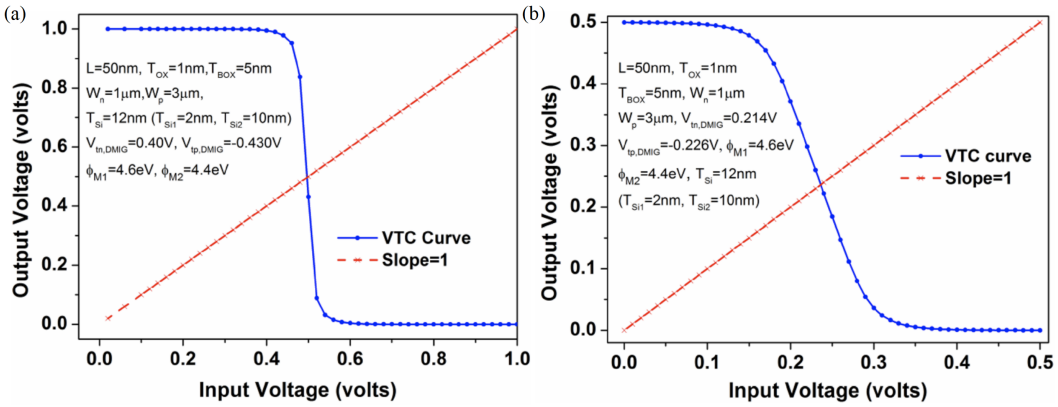

Figure 13. VTC of individual Inverter designed with DMIG FD-SOI MOSFET: (a) at supply voltage = 1 V, (b) at supply voltage = 0.5 V [19]

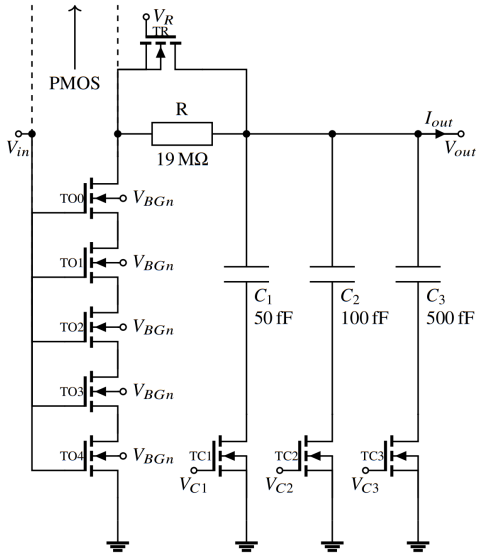

Figure 14. NMOS transistors of one inverter and configurable *R* and *C*1, *C*2 and *C*3 [20]

FD-SOI technology was utilized to provide excellent temperature compensation using the Zero-Temperature Coefficient (ZTC) effect to preserve the oscillator performance in a wide temperature span (Figure 15). Measurement results validated excellent simulation agreement, accompanied by low power and stable frequency, indispensable for wake-up receiver applications in energy-harvesting IoT systems.

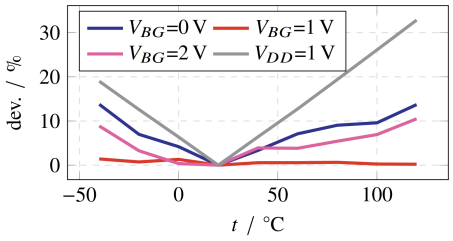

Figure 15. Simulated range of pulse time versus temperature V_{DD}= 0.5 V (colored) compared to V_{DD} = 1 V (Gray) [20]

Together, these illustrations show how process-aware design optimizations such as the application of body biasing in FD-SOI and creative device-level structure design such as DMIG gates enable massive oscillator performance enhancement at the most advanced technology nodes. They also reflect the growing necessity to co-optimize layout, device physics, and digital calibration techniques in an effort to leverage the full benefits of future semiconductor processes.

4. Comparative analysis of design techniques

The below table compares various ultra-low power design techniques for Ring Oscillators in terms of key performance metrics such as power consumption, frequency range, efficiency, and their typical applications (Table 3).

Table 3. Comparative analysis of ultra low power ring oscillator design topologies

Technique	Power consumption	Frequency range	Energy-Per-Cycle (EPC)	Power-Per-GHz (PPG)	Process sensitivity	Typical applications	Implementation and insights
Sub-threshold operation	2.9 pW–few nW	2 Hz	~1.45 nJ/cycle (at 2 Hz, 2.9 pW)	~1.45 µW/GHz	High	Energy-harvesting, biomedical	Extremely low power but highly sensitive to variations of PVT (process, voltage, temperature), very sensitive to calibration for stable operation.
Current-starved inverter	3.75 pW–100s of nW	50 MHz (CSRO), tunable with DTMOS	~75 fJ/cycle (at 50 MHz, 3.75 pW)	~0.075 µW/GHz	Medium	Temperature sensing, IoT timers	Offers programmable delay control, easy integration but tuning precision is highly dependent on control current. Widely used in ultra-low-power SoCs.
Body biasing methods	58.9 nW–100s of nW	2.65 MHz	~22.2 pJ/cycle	~22.2 µW/GHz	Low (with compensation)	Low-power IoT, process-tolerant RO	Allows adaptive threshold tuning to reduce variation effects, moderate complex due to extra bias generation circuits.
Capacitive loading and delay control	0.269 mW	0.890–1.222 GHz	~269 fJ/cycle	~220 µW/GHz	Medium	Digitally tunable PLLs, clock generators	Straightforward design but less effective in leakage control, preferred only when frequency tunability is a higher priority than static power minimization.
Digital calibration and feedback	35 μ W	100–250 MHz	~140 fJ/cycle (at 250 MHz)	~140 µW/GHz	Low	Clocking, wireless baseband, SoCs	Adds digital feedback control for real-time frequency correction, increases PVT robustness but has increased design complexity and area overhead.
Process-aware & technology-optimized designs	<9 nW (FD-SOI), varies with technology node	7 kHz–84.18 GHz	~107 aJ/cycle (at 84.18 GHz)	~0.107 µW/GHz	Low (if tech optimized)	High-frequency ICs, wake-up receivers	Uses node-specific advantages like FD-SOI, FinFET, or back-biasing for extreme energy efficiency, best suited for advanced processes but less portable across technologies.

4.1 *Phase noise and jitter considerations*

Even as power and frequency remain the dominant design parameters for ultra-low power Ring Oscillators (ROs), phase noise and jitter are of equal concern, particularly in communication system-based, clock synchronization, or mixed-signal processing applications. These noise numbers, based on both thermal and flicker noise mechanisms, determine the spectral purity and timing integrity of the oscillator and can have a very significant impact at the system level. In low-power RO design, high timing fidelity is hardest to achieve due to lower bias currents, low signal swing, and the absence of resonant structures that inherently reject noise.

Ring Oscillators at sub-threshold, for instance, are most power-efficient designs but possess very poor phase noise performance. Sub-threshold operation of transistors results in extremely low transconductance and makes the circuit highly sensitive to device mismatch and thermal noise. Thus, sub-threshold ROs are typically beset by high jitter and poor phase noise, limiting their use to non-critical timing applications such as sleep-mode timing or energy-harvesting wake-up clocks for which spectral purity is not of concern.

In contrast, current-starved inverters provide a regulated current path to each inverter stage, enabling fine adjustment of delay while consuming less power. The topology accommodates modest improvement of jitter performance, particularly when paired with Dynamic Threshold MOSFET (DTMOS) biasing, which expands current drive and reduces threshold voltage variation. However, due to their limited slew rates and dependence on stable current mirrors, current-starved oscillators remain moderately jitter-sensitive, particularly under low-voltage operation.

Body biasing techniques, particularly those used in FD-SOI technologies, have even greater scope for jitter minimization. Dynamic control of the threshold voltage of transistors enables body biasing to enhance drive without the associated power increase. Forward body biasing enhances switching speed, thereby reducing rise and fall times of transitions in inverters which are major jitter sources. In particular, self-cascoded body biasing structures have been demonstrated to contain reduced phase noise and increased frequency stability under PVT fluctuations. Such structures are therefore more appropriately used in timing-critical applications such as sensor interfaces and always-on clock generators.

Capacitive tuning methods, usually found on varactors or digitally controlled capacitive arrays, introduce parasitic elements that can affect oscillator linearity and noise performance. Even though the frequency programmability and compact control are made available, the additional load capacitance will shorten signal slew rates and contribute to increased phase noise. Moreover, discrete tuning steps in these circuits could introduce quantization-induced jitter if not properly filtered or averaged.

Digital calibration-based oscillators offer improved jitter control through the application of feedback mechanisms that compensate for delay element variation. Using a reference clock to compare an oscillator output against and digitally correcting delay stages or capacitive loads, these designs can offer reliable frequency operation across process and temperature variability. Though the added logic is subject to reasonable area and power penalty, spectral stability and cycle-to-cycle timing correctness advantage is significant, particularly for digital systems that require tight synchronization.

Process-aware designs such as those due to FD-SOI or FinFET technologies inherently have greater noise immunity due to enhanced electrostatic control and reduced variability. In FD-SOI-based oscillators, independent back-gate biasing not only facilitates strong frequency control but also suppresses flicker noise, one of the greatest phase noise sources in low-frequency designs. These architectures are especially well suited for integration into RF SoCs, wake-up radios, and duty-cycled systems demanding low power consumption and high timing accuracy.

Theses ultra-low power oscillator designs offer varying degrees of integration flexibility and power efficiency, their phase noise and jitter performance must come under close scrutiny when the application is communication-grade or timing-critical (Figure 16). Body biasing and digital calibration techniques offer enhanced performance in this regard, whereas sub-threshold and capacitively-tuned oscillators are best relegated to less noise-sensitive regimes.

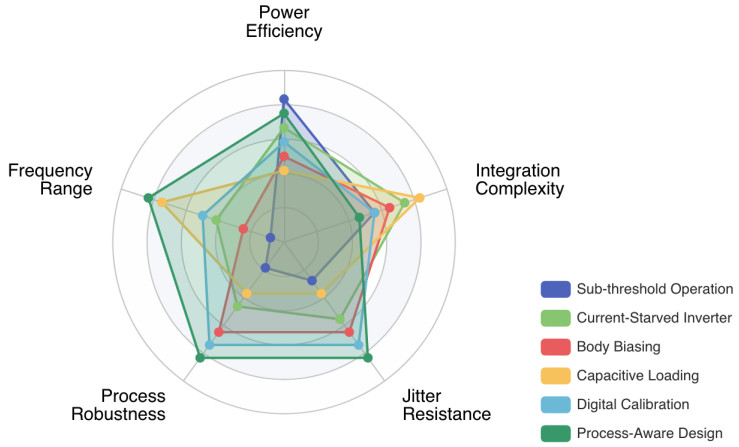

Figure 16. Comparison of ultra-low power Ring Oscillator design techniques across normalized performance metrics

5. Challenges and future directions

Ultra-low power Ring Oscillator (RO) architecture development has helped in tremendous innovation in digital, analog, and mixed-signal domains. However, there are still many challenges that must be overcome, particularly with designers continuing to demand more aggressive power budgets, process nodes, and system-level integrations. Among the most significant is the persistent sensitivity of these circuits to Process, Voltage, and Temperature (PVT) variations. This issue is especially problematic in near-threshold and sub-threshold designs, where the exponential current to threshold voltage relationship aggravates frequency fluctuations between process corners. Even slight ambient temperature changes or supply voltage changes can cause large drift, thereby compromising timing accuracy in long-duration or low-duty-cycle applications.

Achieving frequency stability over environmental conditions is another near-term challenge. Body biasing and digital calibration methods alleviate this to a certain degree, but their feasibility can vary significantly across applications and process technologies. As systems transition to newer nodes such as 7 nm and 5 nm, it becomes increasingly difficult to ensure scalability of oscillator architectures. FinFETs and Gate-All-Around (GAA) technologies, while offering improved leakage and density profiles, can possibly introduce new challenges in analog tunability and layout portability.

Co-design of these oscillators with digital and mixed-signal System-on-Chip (SoC) platforms also demands power domains, noise isolation, and calibration co-design [21]. As demands for low-power timing blocks in always-on systems, energy-harvesting devices, and biomedical implants grow, future designs must balance adaptability, robustness, and ease of integration.

Addressing these challenges will require future work to develop hybridized design styles that combine two or more approaches and leverage their complementary strengths. For example, the integration of body biasing with digital calibration could provide runtime adaptability with low standby power, while the union of process-aware transistor structures with capacitive tuning might provide enhanced agility at the expense of reduced sensitivity to jitter. Also, machine learning in the context of circuit optimization is a robust trend, one that might support modeling non-linear circuit behavior over PVT variations, enable device size via sizing automation, and support on-chip learning-based calibration loops during silicon bring-up.

A key frontier here is application-specific co-design. Rather than seeking global performance improvement, oscillator designs of the next generation need to be targeted specifically to the performance bounds of real systems, for example, energy-harvesting systems, biomedical implants, or wireless sensor nodes. Important design parameters like cold-start

time, duty-cycling behavior, and long-term frequency drift need to come as companions to power efficiency, to allow deployment in harsh or energy-constrained environments.

The community would benefit significantly from an ultra-low power oscillator design common benchmarking methodology. Normalized energy-per-cycle, jitter-to-power envelopes, and temperature stability indices are three standardized measures that would significantly enable cross-comparison and reproducibility. Their inclusion in academic research as well as industrial prototyping would result in more coherent design choices and increase the deployment of laboratory innovations into manufacturable, practical implementations.

6. Conclusion

This paper has presented an overall classification and comparative analysis of existing methods for ultra-low power Ring Oscillator design. There were six major categories that were presented, i.e., sub-threshold operation, current-starved structures, body biasing, capacitive loading, digital calibration, and process-aware design. Each of the methods offers distinct trade-offs between frequency range, power consumption, area, process sensitivity, and implementation complexity.

From the techniques examined for this review, the self-cascoded body biasing and sub-threshold operations seemed to work especially well in ultra-low power consumption, usually in the order of nano to pico-watts. These methods work particularly well when applied to energy-harvesting circuits and biomedical implants where power consumption needs to be kept to an absolute minimum. Their sensitivity to Process, Voltage, and Temperature (PVT) variations themselves create severe challenges to provide reliable operation over manufacturing and environmental variations.

On the other hand, process-aware designs, especially FD-SOI-based technologies, coupled with digitally calibrated Ring Oscillators offer better frequency stability, programmability, and integration flexibility. These characteristics, in turn, make them especially ideal for more complex platforms such as System-on-Chip (SoC) environments where precision and adaptability are critical.

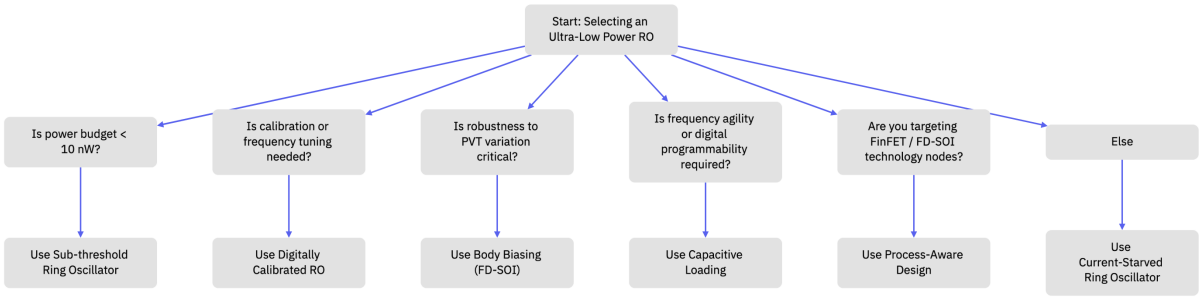

Figure 17. Decision tree of design constraints to suit the design techniques in Ring Oscillators

No single technique can be applied across all applications, and the optimal design style depends heavily on the specific requirements of the target application, whether it be ultra-low power operation, frequency control, small area, or variation immunity (Figure 17). In practice, a hybridisation of methodologies is increasingly being employed, where multiple methods are combined simultaneously to trade off against each other and take advantage of each method's strengths. Future research and applications will likely continue the trend towards highly adaptable, variation-immune, and energy-efficient oscillator structures optimized to the evolving needs of modern electronics.

Conflict of interest

The authors declare no competing financial interest.

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